HITACHI MOS LSI DATA BOOK

LCD DRIVER LSI

INDEX

GENERAL INFORMATION

	Type		General	Segment Display		Character Display			Graphic Display		
LSI Characteristics	Type Number		HD44100H	HD61602	HD61603	HD44780 (LCD-11)	HD44101H	HD43160AH	HD44102CH	HD44103CH	HD61830
	Process		CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS
	Supply Voltage (V)		5*1	3~5*1	3~5*1	5*1	5*1	5*1	5*1	5*1	5*1
	Operating Temperature (°C)		-20~+75*2	-20~+75	-20~+75	-20~+75*2	-20~+75	-20~+75	-20~+75	-20~+75	-20~+75
	Package		FP-60	FP-80	FP-80	FP-80	FP-80	FP-54	FP-80	FP-60	FP-60
	Power Dissipation (mW)		5.0	0.5(5V)	0.5(5V)	1.75	1.75	10.0	2.5	4.0	30.0
Function	Memory	ROM (bits)	-	-	-	7200 (CG)*3	6720 (CG)*3	6240 (CG)*3	-	-	7360 (CG)*3
		RAM (bits)	-	51x4	64x1	80x8/64x8 (CG)*3	32x8	80x8	200x8	-	(external 65536x8)
	I/O	Interface (CPU)	8	14	10	11	12	21	21	6	13
		Interface (Driver IC)	2	-	-	4	4	5	-	5	9
		Interface (External ROM,RAM)	-	-	-	-	-	18	-	-	33
	Number of Instruction		-	4	4	11	8	6	6	-	12
	LCD Driver	Common	40	4	1	16	15	-	-	20	-
		Segment		51	64	40	40	-	50	-	-
		Duty	Free (N)	Static, 1/2,1/3 1/4	Static	1/8,1/11, 1/16	1/7,1/14	1/8,1/12, 1/16	1/8,1/12, 1/16,1/24, 1/32	1/8,1/12, 1/16,1/24, 1/32	1/1 ~ 1/128
		Bias	1/2,1/3, 1/4,1/5	1/2,1/3	-	1/4,1/5	1/4,1/5	-	1/5	1/5	-
	Display Capability		N×40 Matrix (1/N Duty)	204 Segment (1/4 Duty)	64 Segment	16 Digits (5×7 Dots 1/16 Duty)	16 Digits (5×7 Dots 1/14 Duty)	-	32×50 Dots (1/32 Duty)	-	-
Comment			SR type			Expandable to 80 Digits using HD44100H	Expandable to 32 Digits using HD44100H	Display to 80 Digits using HD44100H			Display to 524288 Dots using HD44100H

*1: Except Power Supply for LCD.
*2: -40~+85°C (Special Request). Please contact Hitachi Agents.
*3: CG; Character Generator.

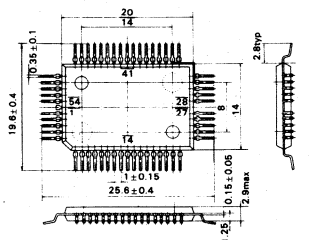
PACKAGING INFORMATION

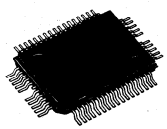
■ PACKAGE INFORMATION

The Hitachi LCD driver devices use plastic flat packages to make more compact the equipment in which they are incorporated and provide higher density mounting by utilizing the features of their thin liquid crystal display elements.

■ PACKAGE INFORMATION (UNIT: mm)

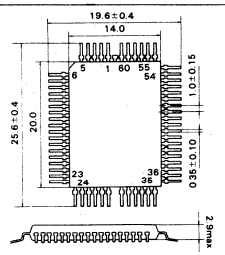
● FP-54

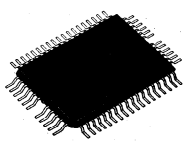




Applicable LSI	HD43160AH

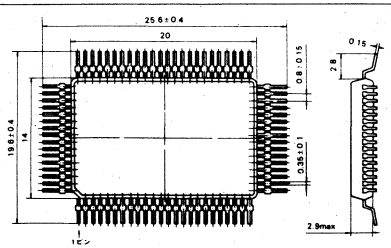
● FP-60

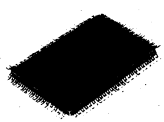




Applicable LSI	HD44100H, HD44103CH, HD61830

● FP-80



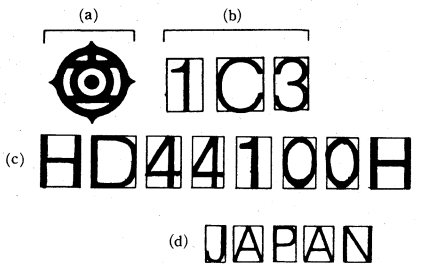


Applicable LSI	HD61602, HD61603, HD44101H, LCD-II(HD44780), HD44102CH

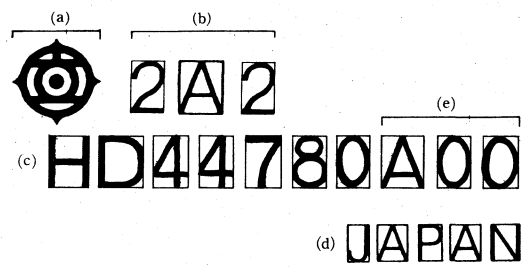
■ MARKING

There are two kinds of marking of the Hitachi LCD driver devices: the one with a standard type No. and the other with a ROM code. The type No. 2 with a ROM code is applied to the HD61830 and LCD II (HD44780).

(1) Standard type No.



(a) Type No. with ROM code



Meaning of each mark

(a)	Hitachi mark
(b)	Lot code
(c)	Standard type No.
(d)	JAPAN mark
(e)	ROM code

RELIABILITY AND QUALITY ASSURANCE

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual user's purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize such quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance moral for quality.

In addition, quality required by users on semiconductor devices is going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.

(2) Build the quality at the sources of manufacturing process.

(3) Execute the harder inspection and reliability confirmation of final products.

(4) Make quality level higher with field data feed back.

(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the

semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices, only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;

- Making clear about fundamental failure mode
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing

2. Effectiveness of evaluation by Test Site are as follows;

- Common fundamental failure mode and failure mechanism in devices can be evaluated.

- Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
- Able to analyze relation between failure causes and manufacturing factors.
- Easy to run tests.

etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competitive power of products, the major purpose of design review is to ensure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.

(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub-program of calculation, experiments, investigation, etc. will be carried out.

(3) Determine contents of reliability and methods, etc. based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Discussion about preparation for production.

(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.

(7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.

(2) Feedback of information should be made to ensure satisfied level of process ability.

(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

(1) The third party performs approval objectively from the standpoint of customers.

(2) Fully consider past failure experiences and information from field.

(3) Approval is needed for design change and work change.

(4) Intensive approval is executed on parts material and process.

(5) Study process ability and fluctuation factor, and set up control points at mass production stage.

Considering the views mentioned above, quality approval shown in Fig. 1 is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are getting higher, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows:

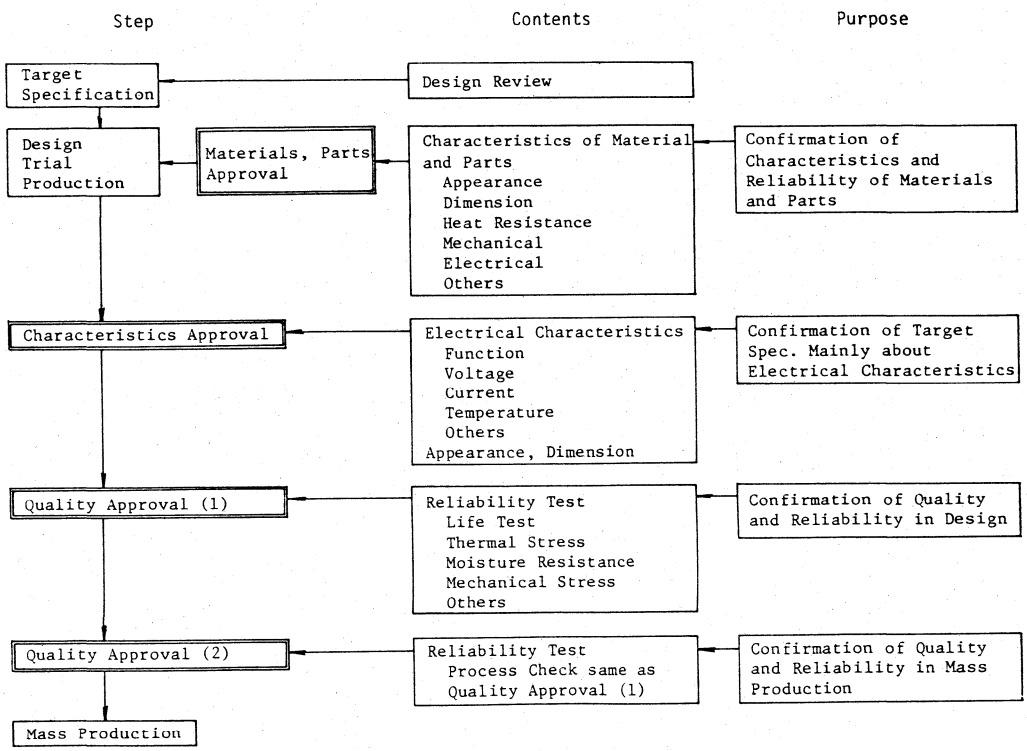


Fig. 1 Flow Chart of Quality Approval

(1) Outside Vendor Technical Information Meeting

(2) Approval on outside vendors, and guidance of outside vendors

(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub-materials. The quality control in the manufacturing process is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and the quality control in the manufacturing process is tightly executed - rigid check in each process and each lot, 100% inspection in appropriate ways to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of counter-measures
- Transmission of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Equipments for manufacturing semiconductor devices have been developing extraordinarily with necessary high performance devices and improvement

of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain proper operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and

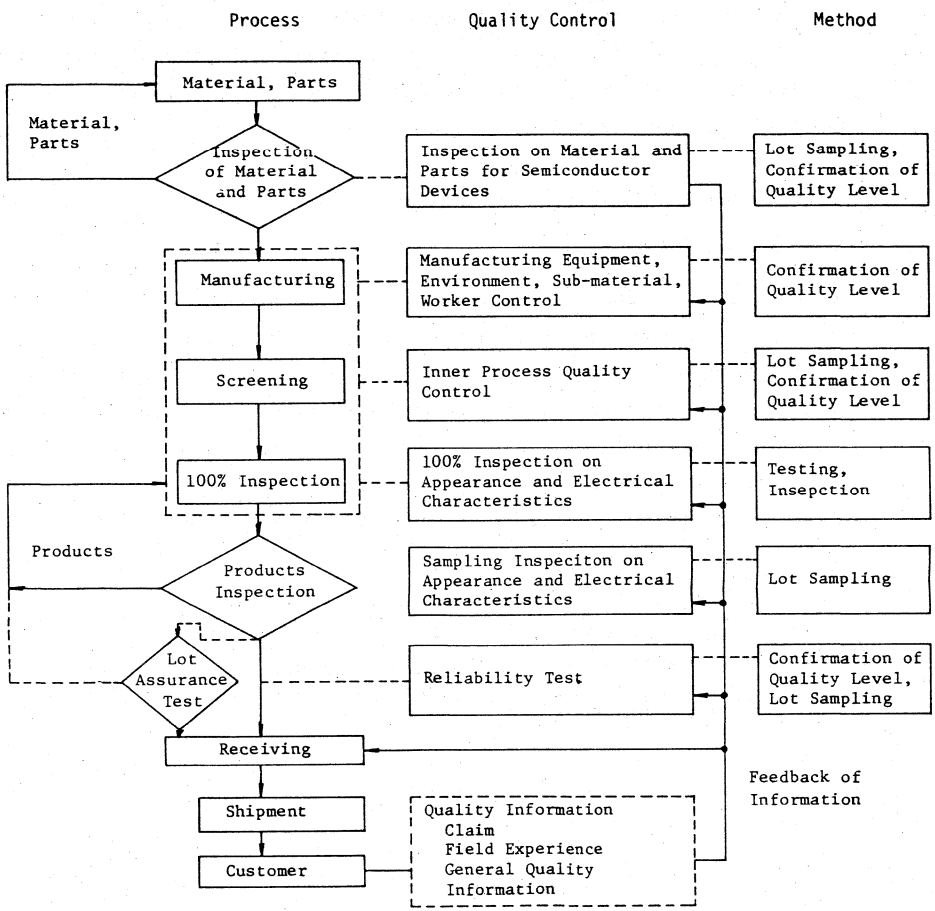


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Submaterials

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufacturing circumstances - temperature, humidity, dust - and the control of submaterials - gas, pure water - used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, airconditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, parts	Important control items	Point for check
Water	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratch
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratch, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratch
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratch
	Dimension	Dimension level
	Leak resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechanical strength
Plastic	Composition	Characteristics of plastic material
	Electrical characteristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

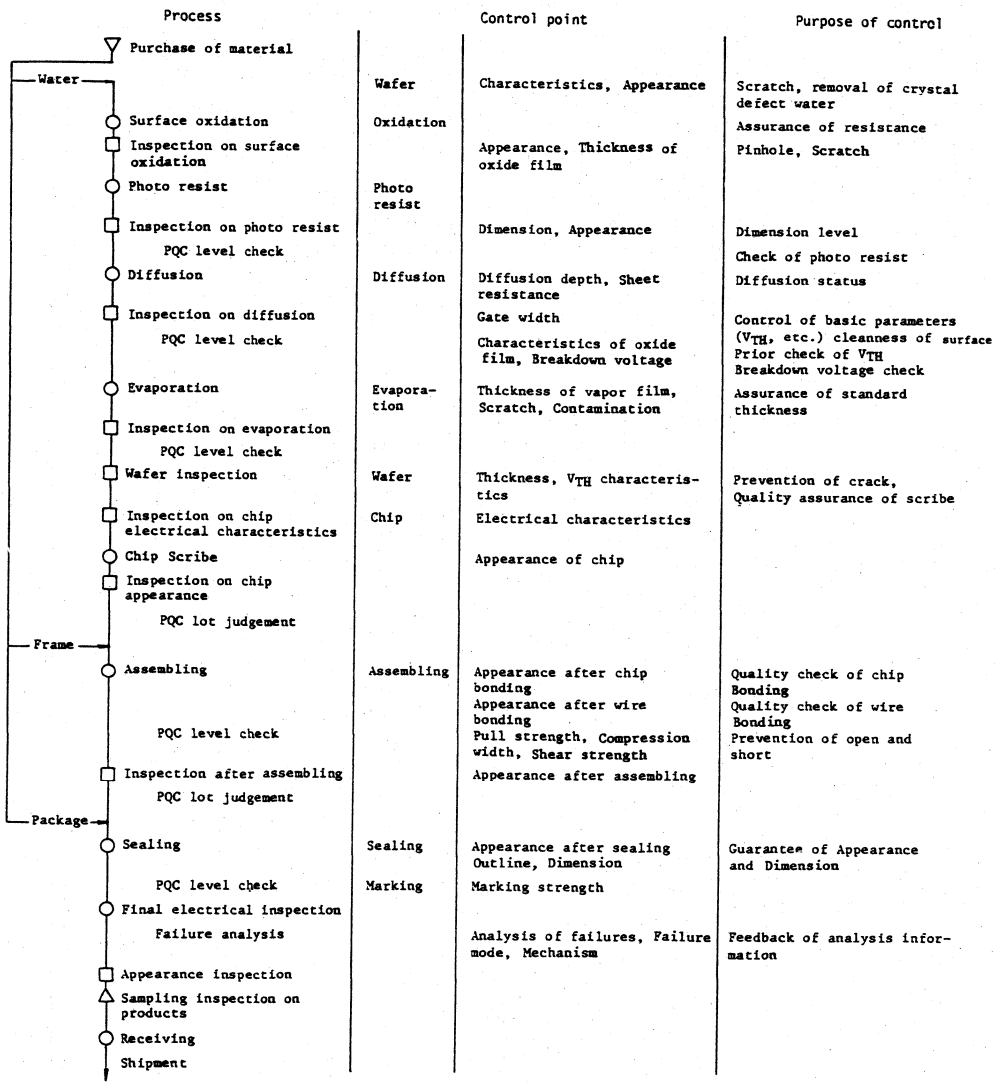


Fig. 3 Example of Inner Process Quality Control

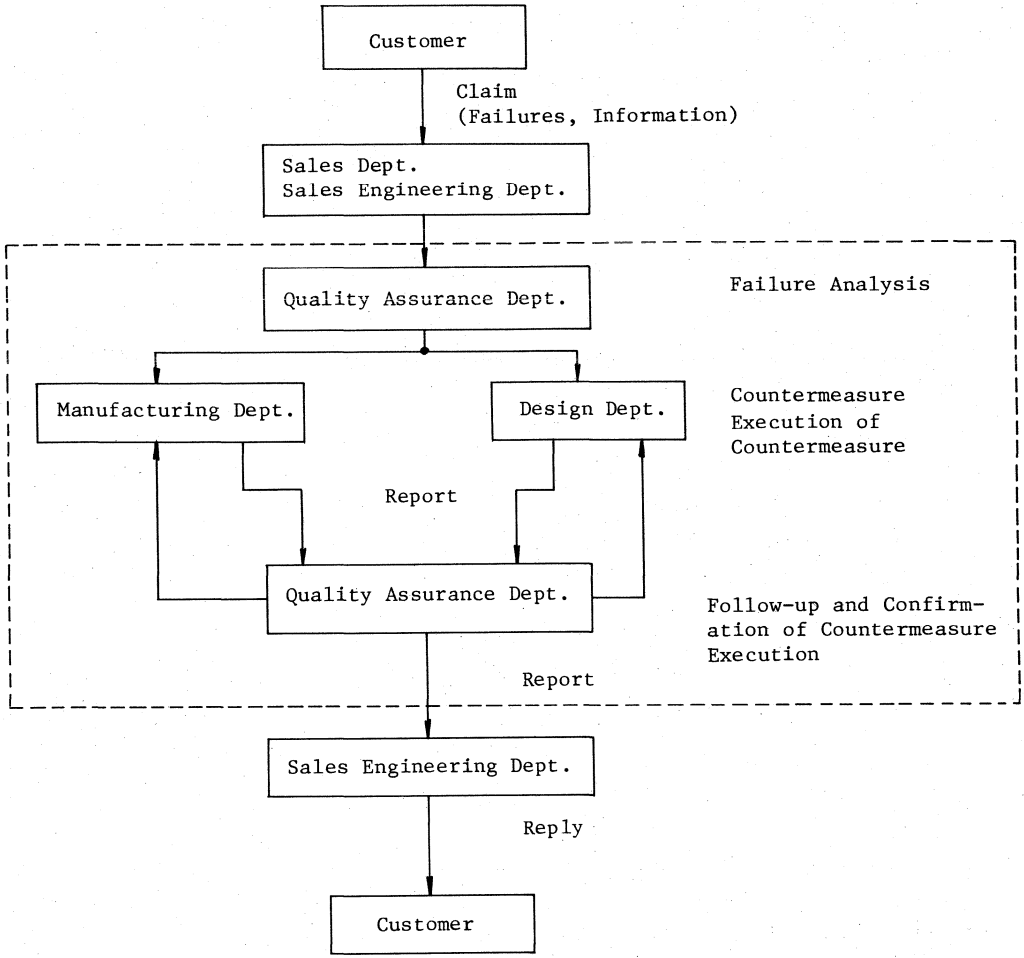


Fig. 4 Process Flow Chart of Field Failure

RELIABILITY TEST DATA OF LCD DRIVERS

1. INTRODUCTION

The use of liquid crystal displays with microcomputer application systems has been increasing, because of their merits such as low power consumption, freedom in display pattern design, and thin shape. Low power consumption and high density packaging have been achieved through the use of the CMOS process and the flat plastic packages, respectively.

This chapter describes reliability and quality assurance data for Hitachi LCD driver LSIs based on test data and failure analysis results.

2. CHIP AND PACKAGE STRUCTURE

Hitachi LCD driver LSI family are produced in low power CMOS technology and flat plastic package. Si-gate process is used for high reliability and high density. Chip structure and basic circuit are shown in Fig. 1, and package structure is shown in Fig. 2.

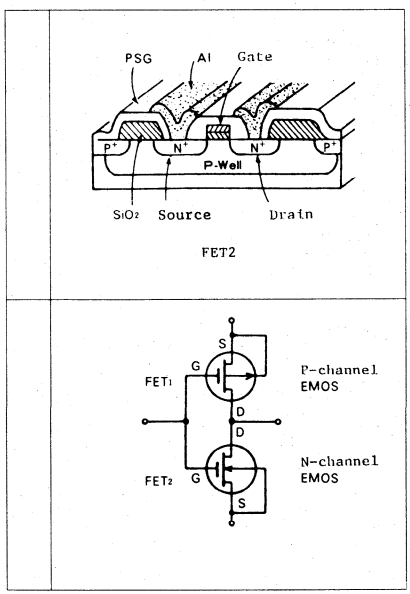


Fig. 1 Chip Structure and Basic Circuit

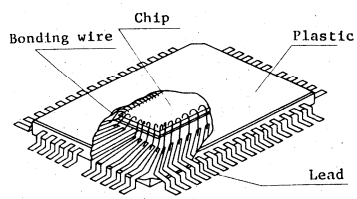


Fig. 2 Package Structure

3. RELIABILITY TEST RESULTS

The test results of LCD Driver LSI family are shown in Table 1, 2 and 3.

Table 1 Test Result (1), High Temperature Operation
(Ta=125°C, V_{CC}=5.5V, V_{EE}=-5.5V)

Device	Sample size	Component hour	Failure
HD44100H	40	40,000	0
HD44101H	40	20,000	0
HD44102CH	40	40,000	0
HD44103CH	40	40,000	0
HD44780	90	90,000	0
Total	250	230,000	0

Table 2 Test Result (2)

Test item	Test condition	Sample size	Component hour	Failure
High temp, storage	Ta=150°C, 1000 hrs.	90	900,000	0
Low temp, storage	Ta=-55°C, 1000 hrs.	80	800,000	0
Steady state humidity	65°C, 95% RH, 1000 hrs.	545	550,000	1*1
Steady state humidity biased	85°C, 90% RH, 1000 hrs.	165	170,000	2*2
Pressure cooker	121°C, 2 ATM. 96 hrs.	55	5,300	0

*1, *2: Aluminum corrosion

Table 3 Test Results (3)

Test items	Test condition	Sample size	Failure
Thermal shock	0 ~ 100°C 10 cycles	108	0
Temperature cycling	-55°C ~ 150°C 10 cycles	678	0
Soldering heat	260°C 10 sec.	132	0
Solderability	230°C 5 sec.	43	0

4. QUALITY DATA FROM FIELD USE

Field failure rate is estimated in advance through production process evaluation and reliability tests. Past field data on similar devices provides the basis for this estimation. Quality information from the users are indispensable to the improvement of products quality. Therefore, field data on products delivered to the users are followed up carefully. On the basis of information furnished by the user, failure analysis is conducted and the results are quickly fed back to the design and production divisions.

Failure analysis result on MOS LSI returned to Hitachi is shown in Fig. 3.

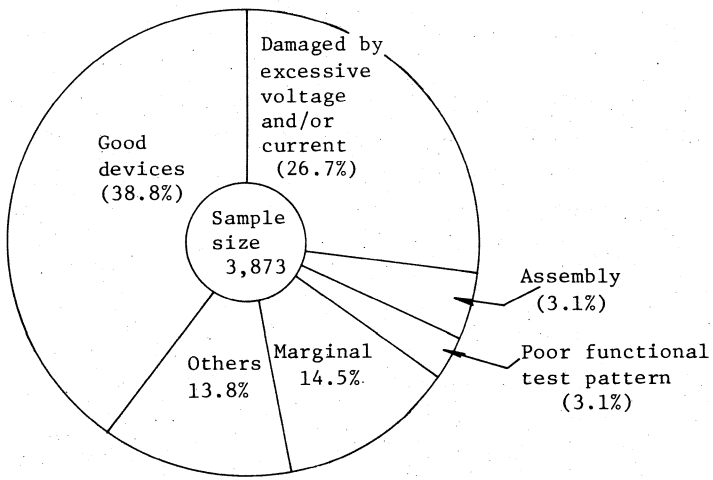


Fig. 3 Failure Analysis Result

5. PRECAUTION

5.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent detrioration in their electrical characteristics, solderability, and appearance, or breakage.

(1) Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.

(2) Store in a clean air environment, free from dust and active gas.

(3) Store in a container which does not induce static electricity.

(4) Store without any physical load.

(5) If semiconductor devices are stored for a long time, store them in the unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.

(6) If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpacked devices must not be stored for over 3 months.

(7) Take care not to allow condensation during storage due to rapid temperature changes.

5.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be given, too:

(1) Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.

(2) In order to prevent device breakage from clothes-induced static electricity, workers should be properly grounded with a resistor while handling devices. The resistor of about 1 M ohm must be provided near the worker to protect from electric shock.

(3) When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a belt conveyor is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.

(4) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

5.3 Handling for Measurement

Avoid static electricity, noise and surge-voltage when semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open to provide the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will fail if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings.

Especially, while the devices are being tested, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source.

During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that no soldering bridge of foreign matter exists before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

FLAT PLASTIC PACKAGE (FPP) MOUNTING METHODS

The FPP can obtain better space factors than DIP type because the board occupying area and thickness can be reduced. No through holes nor lead forming is required for mounting the board. Therefore, the FPP can be mounted as it is, and is suitable for automatic mounting, providing remarkable reduction of manpower.

Various mounting methods are provided and can be used for each purpose. The typical example of mounting are given below.

1. Individual Mounting with Soldering Iron

   A method used mainly in the trial and small-scale production of circuits. The FPP can be soldered by fixing it on the mounting part of the printed circuit board with flux or adhesive agent while pressing it. For mounting, sharpen the tip of soldering iron or make it in a block shape so that more than one pin can be heated simultaneously. Use a fine solder (about ϕ 0.5mm). Solder within 10 seconds per IC at the maximum temperature of 260°C for lead and 235°C for resin part (lead bottom) as the heating conditions.

2. Reflow Soldering

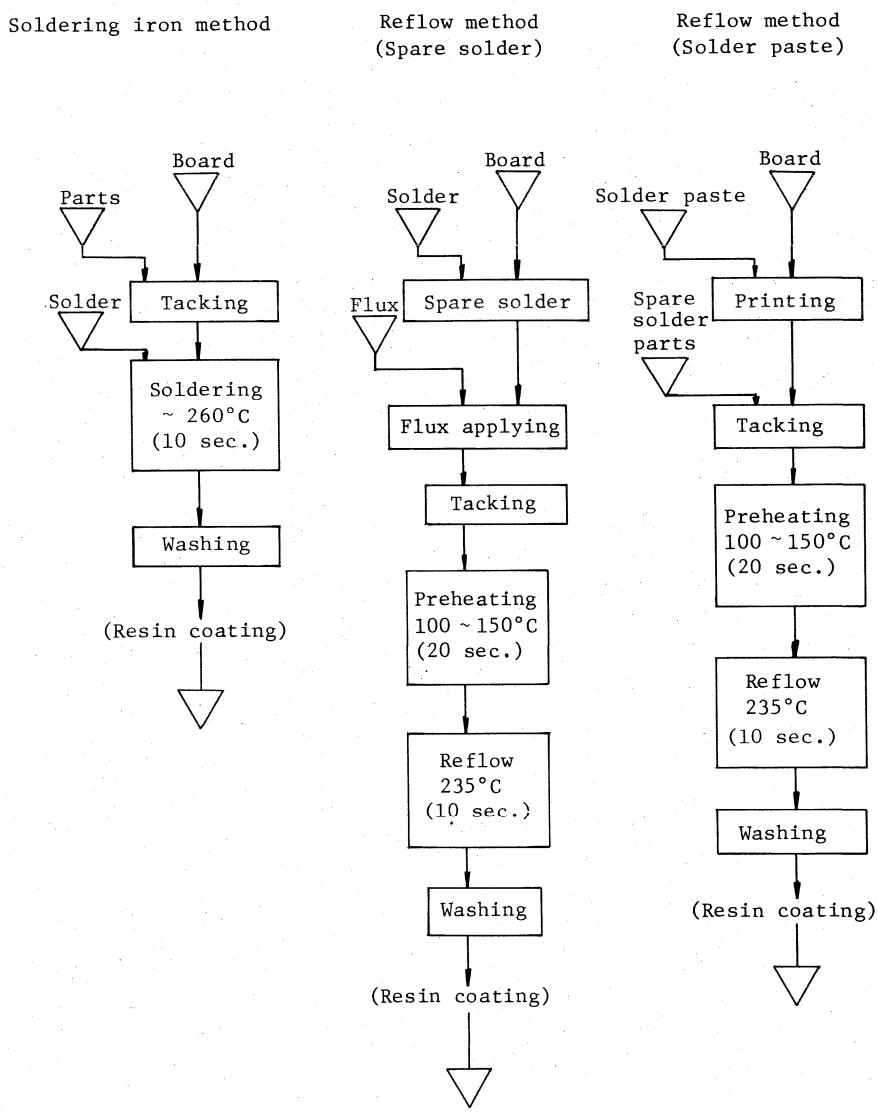
   The reflow soldering is the most general method in which the chips such as a transistor, a resistor and a capacitor are mounted on a hybrid IC. It can be also applied to the FPP. (Note) In addition, there are methods in which spare soldering and flux are applied to a printed circuit board in advance and in which solder paste is selectively applied to a printed circuit board by screen process printing.

   The FPP is tacked at a specified position with flux or solder paste. However, a small amount of adhesive can be applied to the rear of FPP for temporary fixing. Spare solder is melted by passing the board whose parts are tacked, through a temperature-controlled hot plate or conveyor type heater. Then the board can be soldered. In this case, preheat thoroughly to eliminate the thermal distortion of board and mounted parts. Pay attention to temperature control in consideration of the heat absorption of black plastic caused by an infrared-ray heater. As the heating conditions, preheat the board and parts for 20 seconds at a temperature of 100 to 150°C. Then heat them within 10 seconds at the maximum temperature of

235°C as a resin surface temperature . If the board is directly heated from the upper side of FPP with an infrared-ray heater, the temperature of resin surface becomes higher than the lead. Therefore, a shielding plate or similar thing must be used so that the temperature of resin surface can be 235°C or below.

(Note) Reflow soldering can be applied to the 2.9 mm (Max.) thick FPP used in the LCD driver series. However, the FPPs of 2.4 mm (Max.) and 1.5 mm (Max.) in thickness cannot be used for reflow soldering under the above conditions.

Flowcharts of Mounting Methods



Driving a liquid crystal at direct current triggers electrode reaction inside the liquid cell, deteriorating display quality rapidly. The liquid crystal must be driven at alternating current. The AC driving method includes the static driving method and the multiplex driving method, each of which has the features and can be used for applications. Hitachi has been developping the LCD driver devices corresponding to the static driving method and the multiplex driving method. The following sections describe the features of each driving method, the driving waveforms and how to apply bias.

STATIC DRIVING METHOD

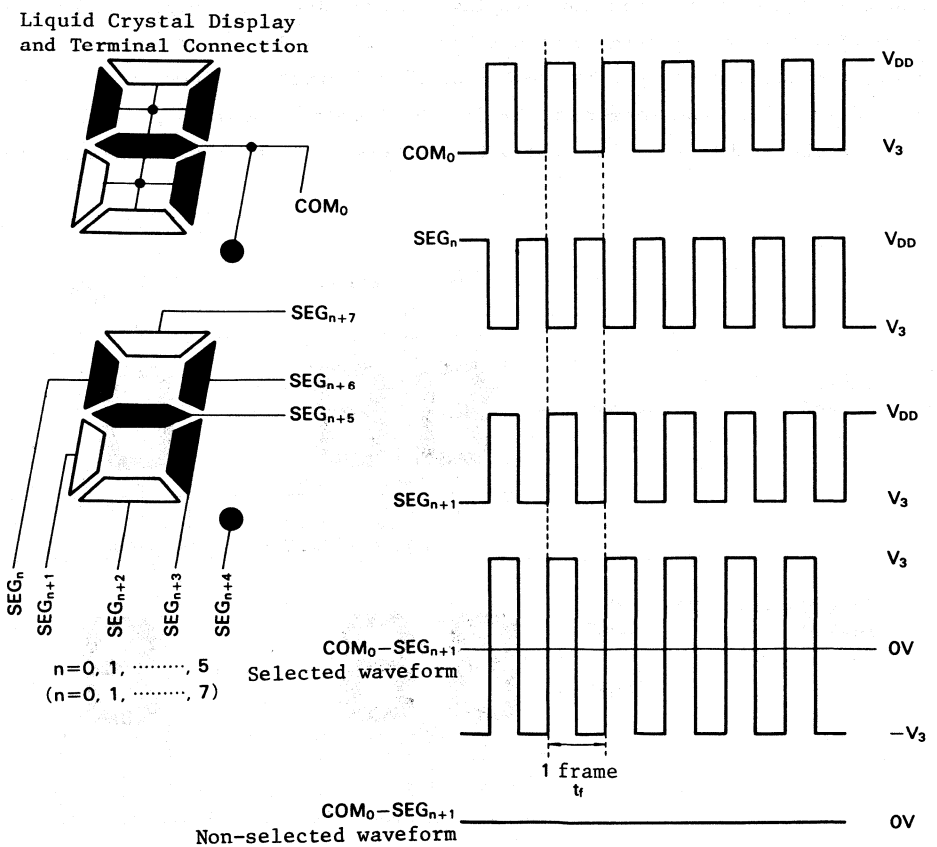


Fig. 1 Example of Static Drive Waveforms
(Example of HD61602/HD61603)

Fig. 1 shows the driving waveforms of the static driving method and an example in which "4" is displayed in the segment method. The static driving method is the most basic method in which good display quality can be obtained. However, it is not suitable for the display of the liquid crystal with many segments because one liquid crystal driver circuit is required per segment. The static driving method is used at the frame frequency ($1/t_f$) of several tens to several hundreds Hz.

MULTIPLEX DRIVING METHOD

The multiplex driving method is effective in reducing the number of driver circuits, the number of connections between the circuit and the display cell, and the cost when driving many display picture elements. Fig. 2 shows the comparision of the static drive with the multiplex drive (1/3 duty) in 8-digit numeric display. The number of liquid crystal driver circuits required is 65 for the former and 27 for the latter. The multiplex drive reduces the number of driver circuits. However, the more multiplexed, the

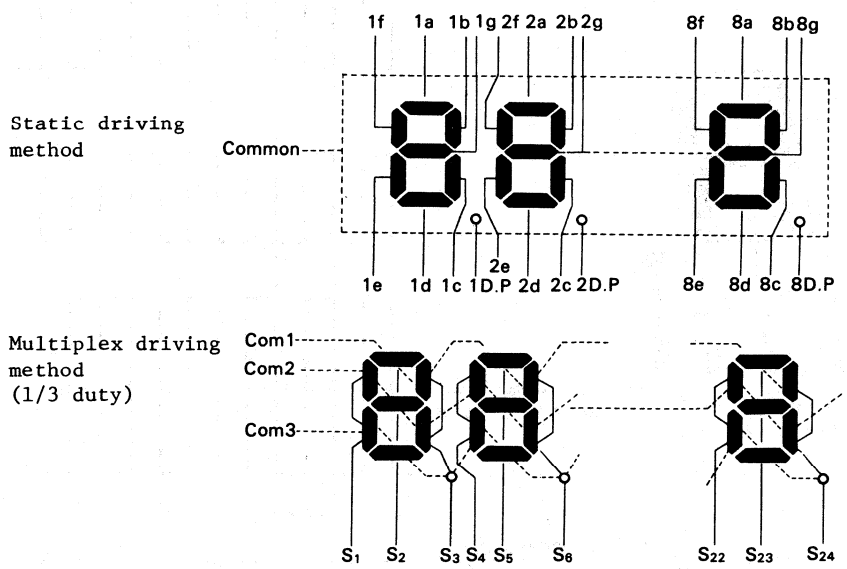


Fig. 2 Example of Comparision of Static Drive with Multiplex Drive

smaller the driving voltage tolerance. Thus, there are limits to extent of multiplexing.

There are two types of multiplex drive waveforms: A type and B type. A type, shown in Fig. 3, is used for alternation in 1 frame. B type is used for alternation in between 2 frames. B type has better display quality than A type in high multiplex drive.

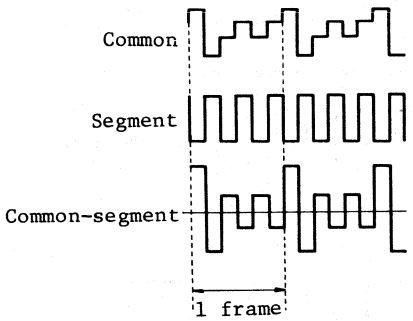


Fig. 3 A Type Waveforms
(1/3 duty, 1/3 bias)

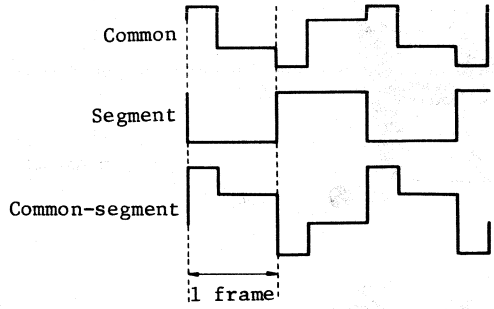


Fig. 4 B Type Waveforms
(1/3 duty, 1/3 bias)

● 1/2 Bias, 1/2 Duty Drive

In the 1/2 duty drive, 1 driver circuit drives 2 segments. Fig. 5 shows an example of the connection in displaying '4' on the liquid crystal display of 7-segment type, and the output waveforms.

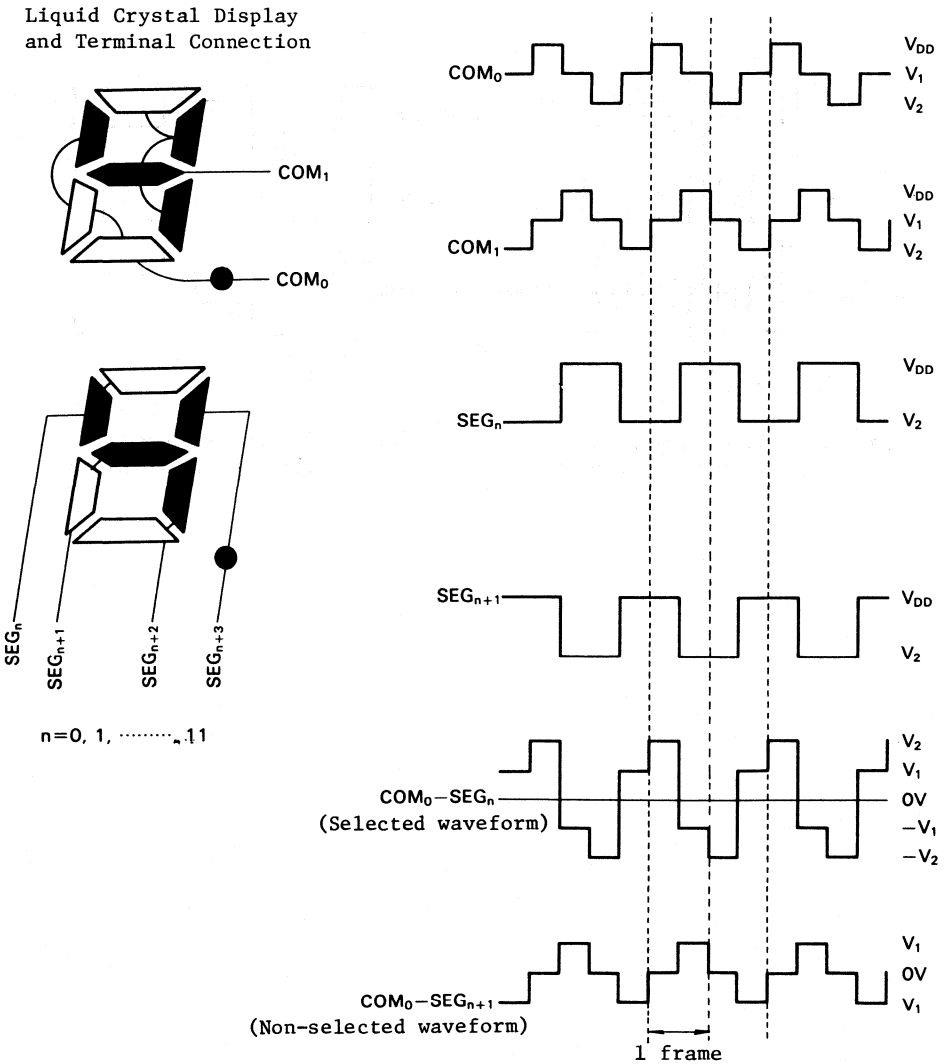


Fig. 5 Example of Waveforms in 1/2 Duty Drive (B type)
(Example of HD61602)

● 1/3 Bias, 1/3 Duty Drive

In the 1/3 duty drive, 3 segments are driven by 1 segment output driver. Fig. 6 shows an example of the connection in displaying '4' on the liquid crystal display of 7-segment type, and the output waveforms.

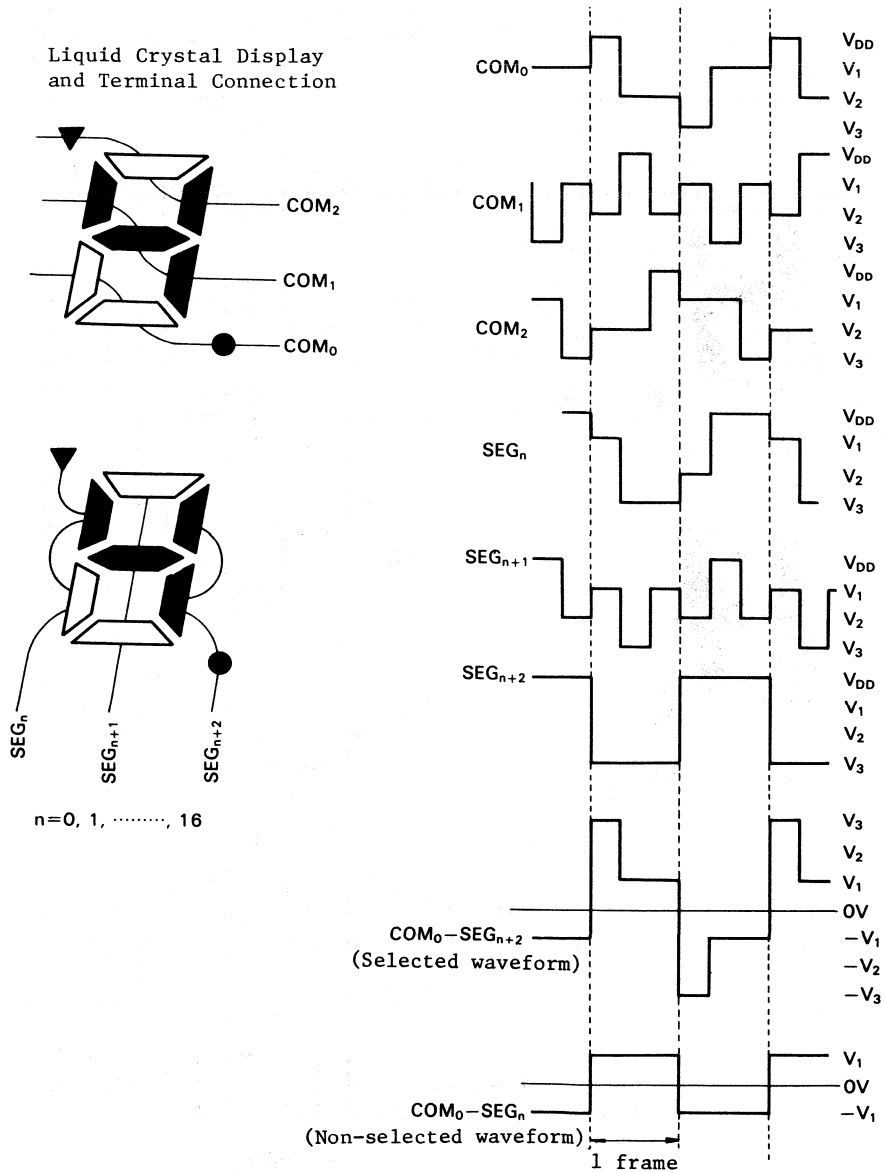


Fig. 6 Example of Waveforms in 1/3 Duty Drive (B type)
(Example of HD61602)

● 1/3 Bias, 1/4 Duty Drive

In the 1/4 duty drive, 4 segments are driven by 1 segment output driver. Fig. 7 shows an example of the connection in displaying '4' on the liquid crystal of 7-segment type, and the output waveforms.

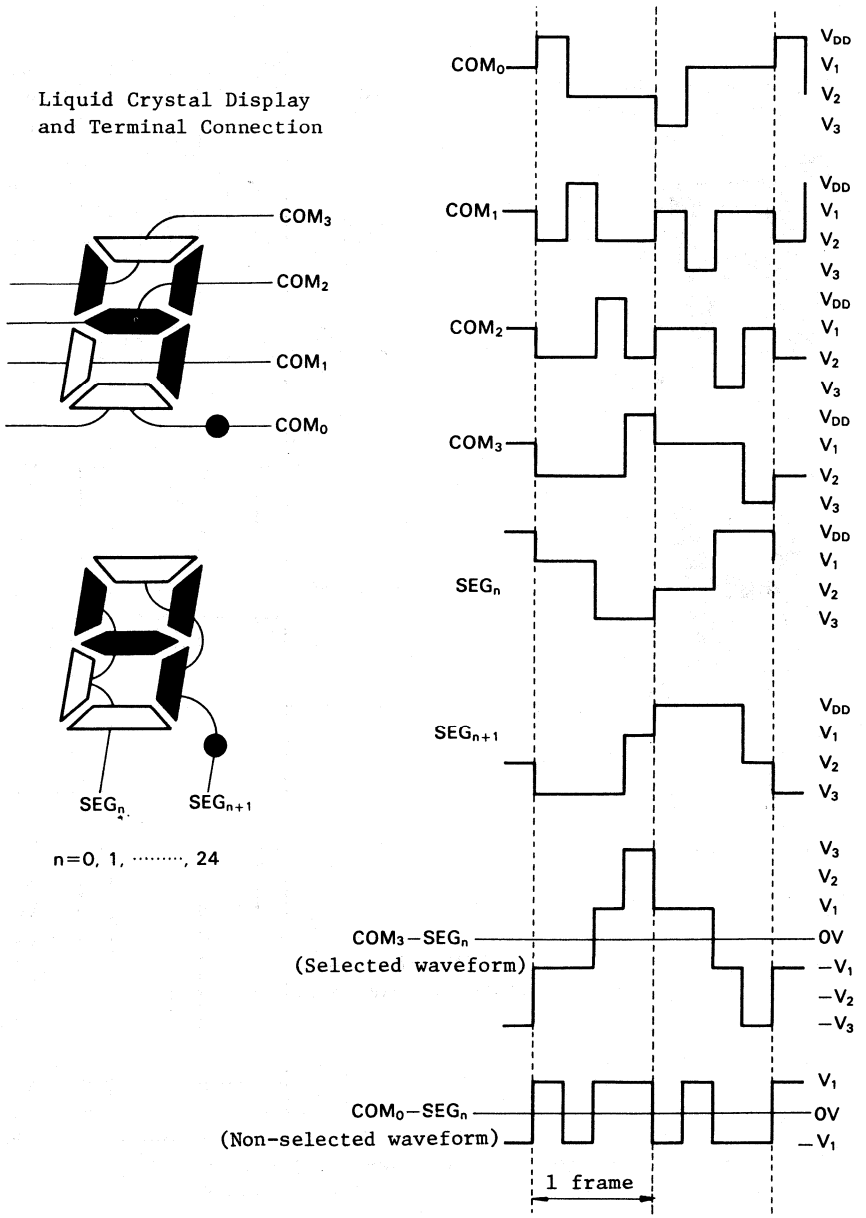
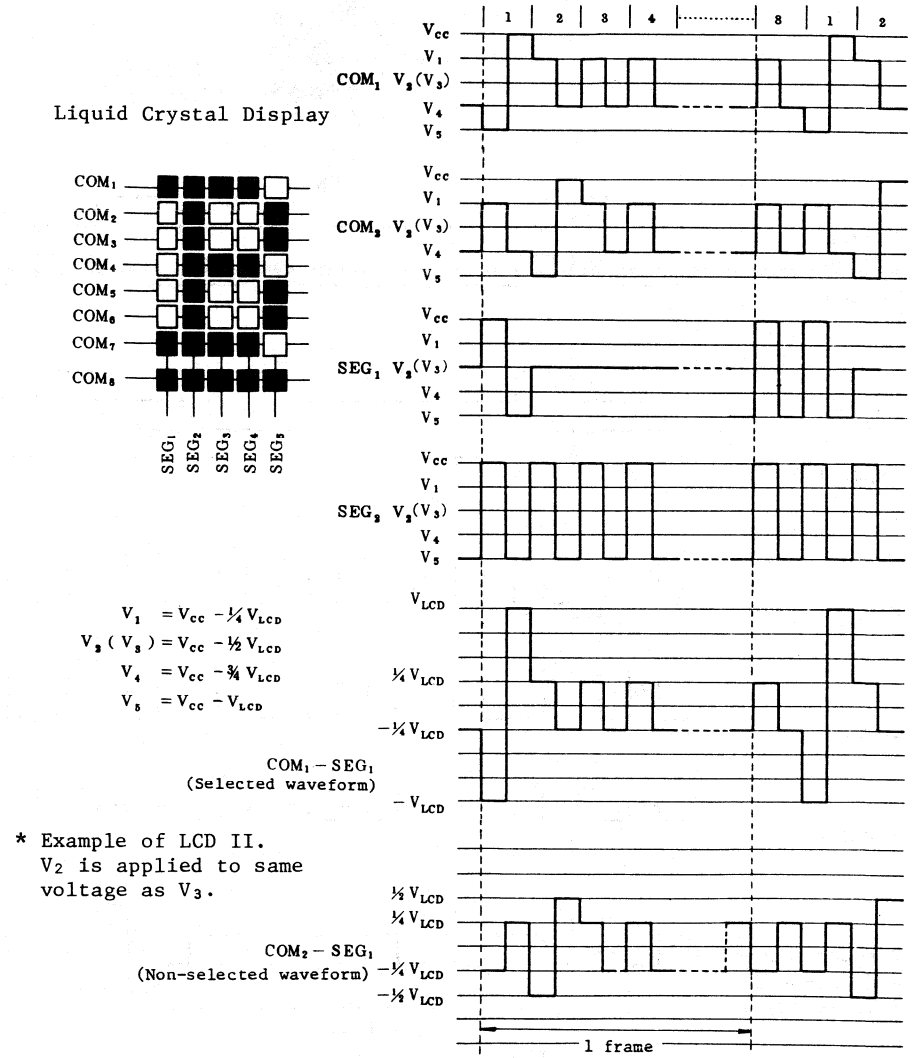


Fig. 7 Example of Waveforms in 1/4 Duty Drive (B type)
(Example of HD61602)

● 1/4 Bias, 1/8 Duty Drive



* Example of LCD II.
V_2 is applied to same voltage as V_3.

Fig. 8 Example of Waveforms in 1/8 Duty Drive (A type)
(Example of LCD-II)

● 1/5 Bias, 1/8 Duty Drive

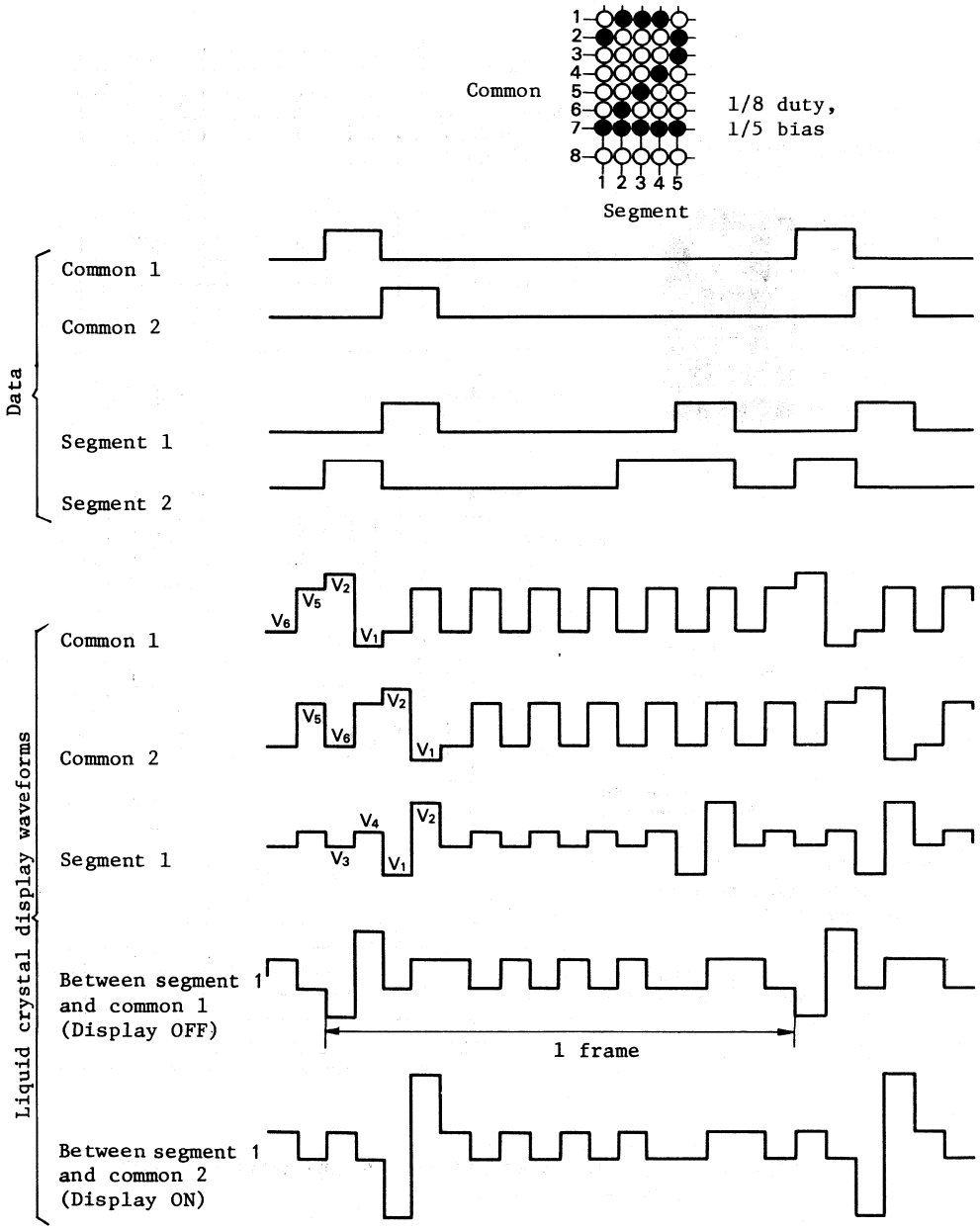


Fig. 9 Example of Waveforms in 1/8 Duty Drive (A type)
(Example of HD44100H)

● 1/5 Bias, 1/16 Duty Drive

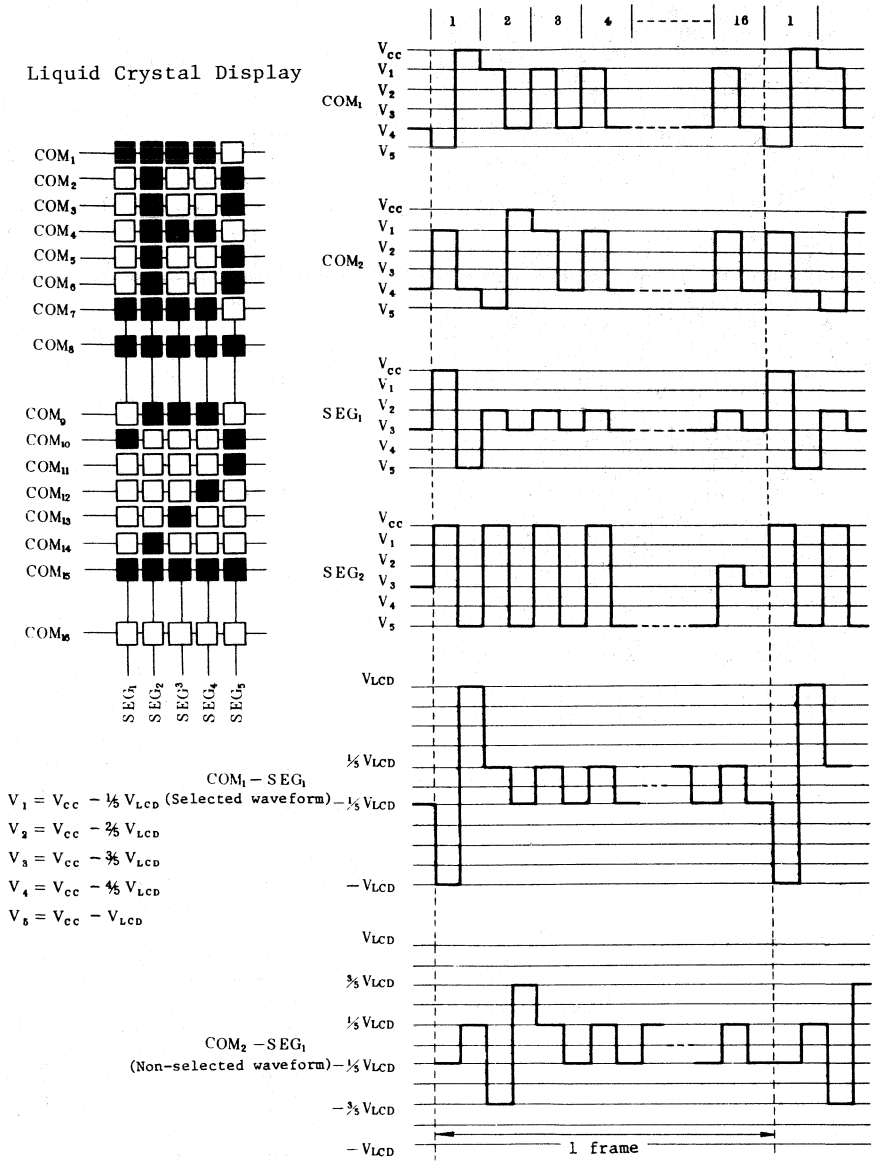


Fig. 10 Example of Waveforms in 1/16 Duty Drive (A type)
(Example of LCD-II)

● 1/5 Bias, 1/32 Duty Drive

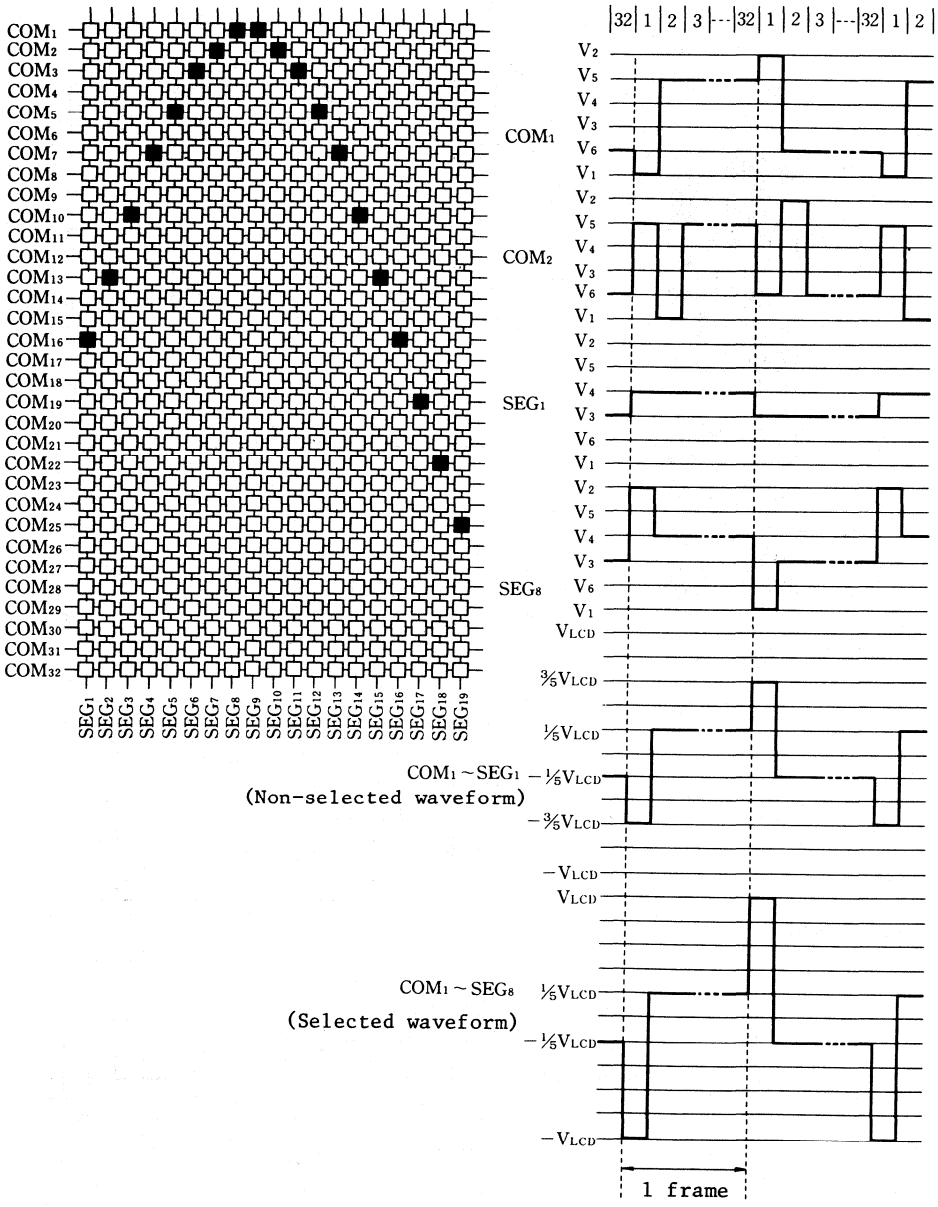


Fig. 11 Example of Waveforms in 1/32 Duty Drive
(Example of HD44102CH, HD44103CH)

■ POWER SUPPLY CIRCUIT FOR LIQUID CRYSTAL DRIVE

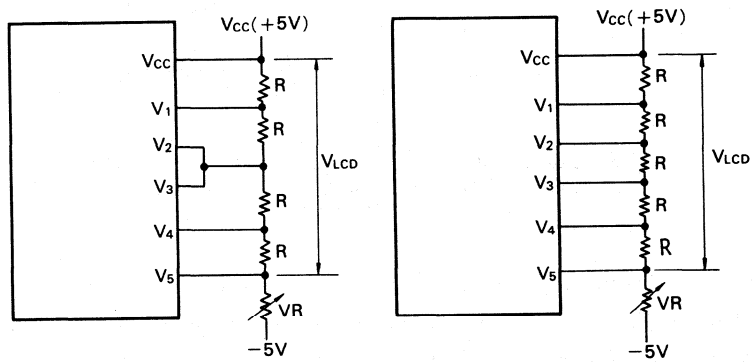
Table 1 shows the relationship between the number of driving biases and display duty ratios.

Table 1 Relationship between the Number of Dispaly Duties Ratio and the Number of Driving Biases

Display duty ratio	Static	1/2	1/3	1/4	1/7	1/8	1/11	1/12	1/14	1/16	1/24	1/32	1/64
Number of driving biases	2	3 (1/2 bias)	4 (1/3 bias)		5 (1/4 bias)				6 (1/5 bias)				

● Drive in Resistance Dividing

A driving bias is generally generated in resistance dividing.



(a) 1/4 Bias (1/8, 1/11 duty) (b) 1/5 Bias (1/16 duty)

Fig. 12 Example of Driving Voltage Supply

The setting of resistance value is determined by considering of operation margine and power consumption. Since the liquid crystal display load is capacitive, the drive waveform itself is distorted due to charge/discharge current when the liquid crystal display drive waveform is applied. To reduce distortion, the resistance value should be decreased but the power consumption increases because of the increase of the current through the dividing resistors. Since larger liquid crystal display panels have larger capacitance, the resistance value must be decreased.

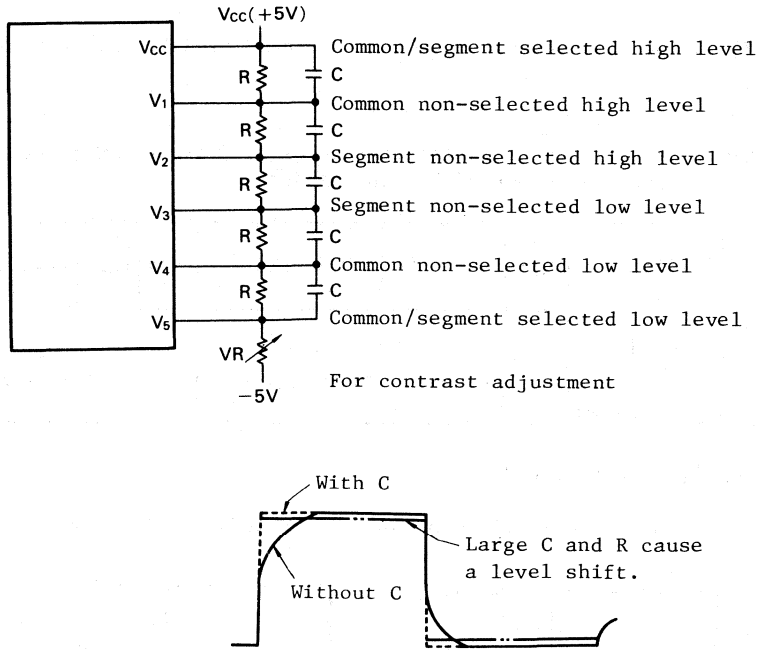


Fig. 13 Example of Capacitor Connection for Improvement of Liquid Crystal Display Drive Waveform Distortion (1/5 bias) (Example of LCD-II)

It is efficient to connect a capacitor to the resistors in parallel as shown in Fig. 13 in order to improve charge/discharge distortion. However, the effect is limited. Even if it is attempted to reduce the power consumption with a large resistor and improve waveform distortion with a large capacitor, a level shift occurs and the operating margine is not improved.

Since the liquid crystal display load is of matrix configuration, the path of the charge/discharge current through the load is complicated. Moreover, it varies depending on display condition. Thus, a value of resistance cannot be simply determined from the load capacitance of liquid crystal display. It must be experimentally determined according to the demand for the power consumption of the equipment in which the liquid crystal display is incorporated.

Generally, R is 1kΩ to 10kΩ, and VR is 5kΩ to 50kΩ. No capacitor is used. A capacitor of 0.1μF is usually used if necessary.

● Drive by Operational Amplifier

In graphic display, the size of liquid crystal becomes larger and the display duty ratio becomes smaller, then the stability of liquid crystal drive level is more important than small display system.

Since the liquid crystal for graphic display is large and has many picture elements, the load capacity becomes large. The high impedance of the power supply for liquid crystal drive produces distortion in the drive waveforms, and deteriorates display quality. For this reason, the liquid crystal drive level should be low impedance with operational amplifiers. Fig. 14 shows an example of operational amplifier configuration.

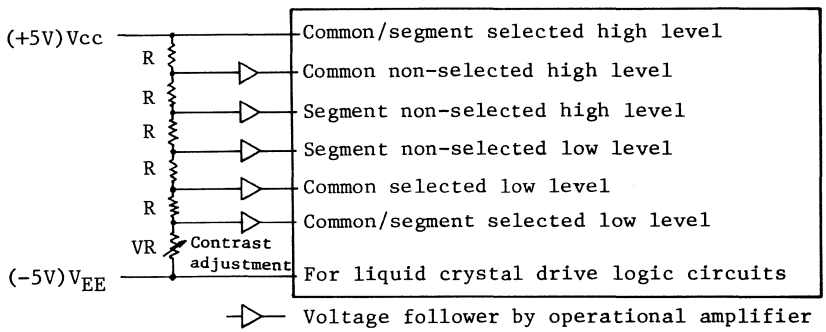


Fig. 14 Drive by Operational Amplifier (1/5 bias)

No load current flows through the dividing resistors because of the high input impedance of operational amplifier. A high resistance of R = 10kΩ and VR = 50kΩ can be used.

● Generation of Liquid Crystal Drive Level in LSI

The power supply circuit for liquid crystal drive level may be incorporated in the LSI such as for portable calculator with liquid crystal display.

HD61602, HD61603 for small display system has built-in power supply circuit for liquid crystal drive level.

DATA SHEETS

● Precaution on Power Supply Circuit

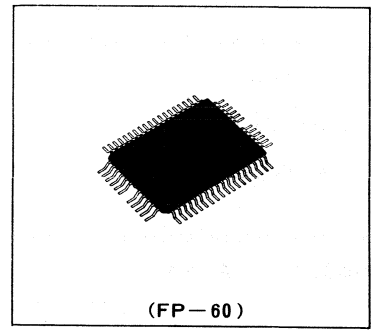
The LCD driver LSI has two types of power supplies: the one for logical circuits and the other for liquid crystal display drive circuit. The power supply system is complicated because of several liquid crystal drive levels.

For this reason, in the power supply design, take care not to deviate from the voltage range assured in the maximum rating at the rise of power supply and from the potential sequence of each power supply. If the input terminal level is indefinite, through current flows and the power consumption increases because of the use of CMOS process in the LCD driver. Simultaneously, the potential sequence of each power supply becomes wrong, and a latch-up phenomenon may be caused.

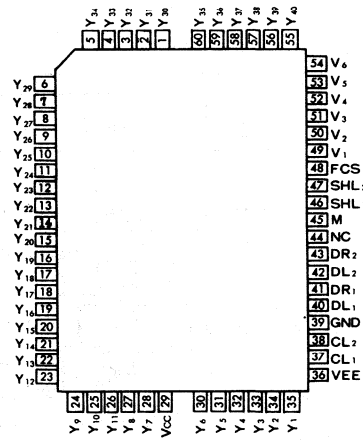
HD44100H (LCD DRIVER WITH 40-CHANNEL OUTPUTS)

The HD44100H has two sets of 20-bit bidirectional shift registers, 20 data latch flip flops and 20 liquid crystal display driver circuits. It receives serial display data from a display control LSI, converts it into parallel data and supplies liquid crystal display waveforms to the liquid crystal.

The HD44100H is a liquid crystal display driver with high generalizability, which can drive a static drive liquid crystal and a dynamic drive liquid crystal, and can be applied to a common driver or segment driver.



PIN ARRANGEMENT



(Top View)

■ FEATURES

- Liquid crystal display driver with serial/parallel conversion function
- Serial transfer facilitates board design
- Capable of interfacing to liquid crystal display controllers: HD43160AH, LCTC (HD61830), HD44101H, LCD Ⅱ(HD44780), LCDⅢ (HD44790).
- Internal liquid crystal display driver ... 40 drivers
- Internal serial/parallel conversion circuits
  20-bit shift register × 2
  20-bit data latch × 2
- Display bias: Static ∿ 1/5

- Power supply

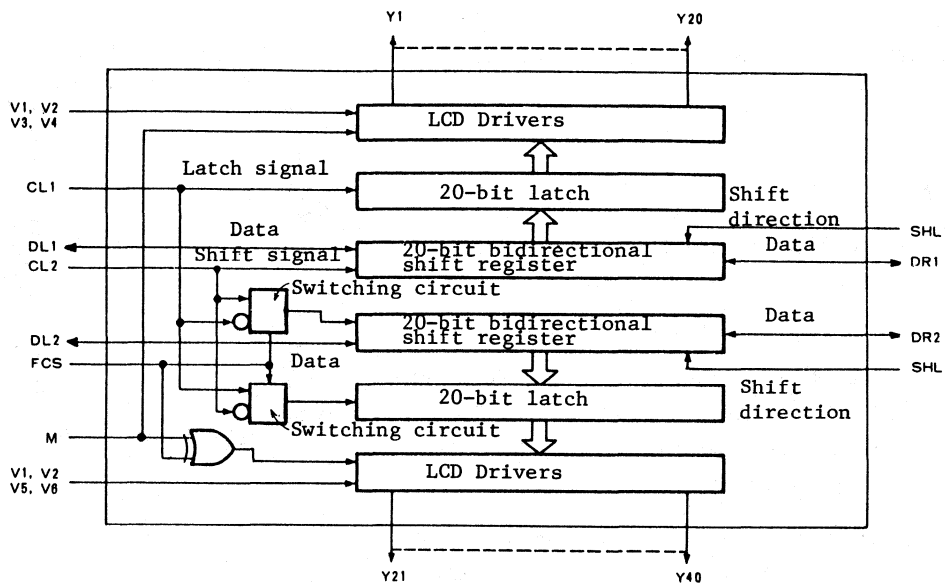
  Internal logic: +5V

  Liquid crystal display driver circuit: -5V

  The separation of internal logic from liquid crystal display driver circuit allows applicable controllers and liquid crystal types to increase.

- CMOS process
- 60-pin flat plastic package

■BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Value	Unit
Supply voltage	Logic	V_{CC}	- 0.3 to +7.0	V *1
	LCD drivers	V_{EE} *2	V_{CC} - 13.5 to V_{CC} + 0.3	V
Input voltage		V_{T1}	- 0.3 to V_{CC} + 0.3	V *1
Input voltage		V_{T2} *3	V_{CC}+0.3 to V_{EE}-0.3	V
Operating temperature		T_{opr}	- 20 to +75	°C
Storage temperature		T_{stg}	-55 to +125	°C

*1 All voltage values are referenced to GND.

*2 Connect a protection resistor of 220Ω ± 5% to V_{EE} power supply in series.

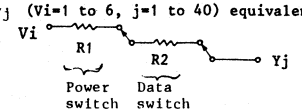
*3 Applies to V_1 to V_6

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, V_{EE} = -5V ± 10%, GND = 0V, Ta = -20 to + 75°C)

Item	Symbol	Applicable terminal	Test condition	min	typ	max	Unit
Input voltage	V_{IH}	CL1,CL2,DL1,DL2,DR1,DR2, M,SHL1,SHL2,FCS		0.7 V_{CC}	-	V_{CC}	V
	V_{IL}			0	-	0.3 V_{CC}	V
Output voltage	V_{OH}	DL1,DL2,DR1,DR2	I_{OH} = -0.4mA	V_{CC} - 0.4	-	-	V
	V_{OL}		I_{OL} = +0.4mA	-	-	0.4	V
Vi-Yj voltage descending	V_{D1}	*1	I_{ON} = 0.1mA for one of Yi	-	-	1.1	V
	V_{D2}		I_{ON} = 0.05mA for each Yi	-	-	1.5	V
Input leakage current	I_{IL}	CL1,CL2,DL1,DL2,DR1,DR2, M,SHL1,SHL2,FCS,NC	Vin = 0 to V_{CC}	-5.0	-	5.0	µA
Vi leakage current	I_{VL}	*3	V_{in} = V_{CC} to V_{EE}	-10.0	-	10.0	µA
Power supply current	I_{CC}	*2	f_{CL2} = 400kHz	-	-	1.0	mA
	I_{EE}		f_{CL1} = 1kHz	-	-	10	µA

*1 Vi - Yj (Vi=1 to 6, j=1 to 40) equivalent circuit



R1= 1kΩ typ.
R2=10kΩ typ.

*2 Input/output current is excluded; when input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

*3 Output Y1 to Y40 open.

■ TIMING CHARACTERISTICS
(V_{CC} = 5V ± 10%, V_{EE} = -5 ± 10%, GND = 0V, Ta = -20 to + 75°C)

Item		Symbol	Applicable terminal	Test condition	min	typ	max	Unit
Data shift frequency		fCL	CL2		-	-	400	kHz
Clock width	High level	tCWH	CL1,CL2		800	-	-	ns
	Low level	tCWL	CL2		800	-		ns
Data set-up time		tSU	DL1,DL2,DR1,DR2,FLM		300	-	-	ns
Clock set-up time		tSL	CL1,CL2	(CL2→CL1)	500	-	-	ns
Clock set-up time		tLS	CL1,CL2	(CL1→CL2)	500	-	-	ns
Data delay time		tpd	DL1,DL2,DR1,DR2	C_L = 15 pF	-	-	500	ns
Clock rise/fall time		tct	CL1,CL2		-	-	200	ns

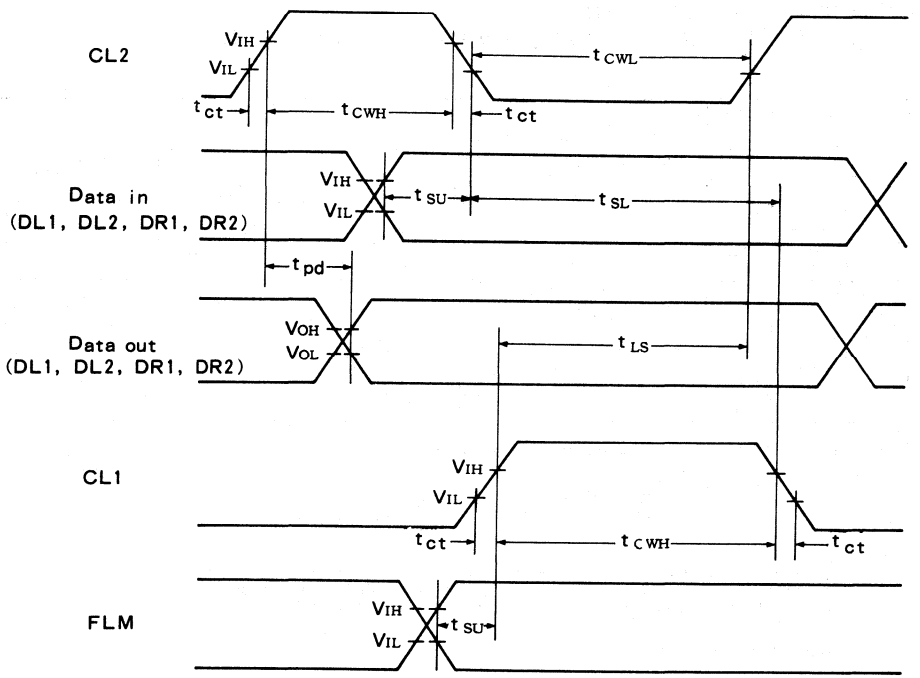


Fig. 1 Timing Waveform

■ TERMINAL FUNCTION

Table 1 Fucntional Description of Terminals

Signal name	Number of lines	Input/ Output	Connected to	Function
V_{CC}	1		Power supply	Power supply for logical circuit
GND	1		Power supply	0V
V_{EE}	1		Power supply	Power supply for liquid crystal display drive
$Y_1 \sim Y_{20}$	20	Output	Liquid crystal	Liquid crystal driver output (Channel 1)
$Y_{21} \sim Y_{40}$	20	Output	Liquid crystal	Liquid crystal driver output (Channel 2)
V_1, V_2	2	Input	Power supply	Power supply for liquid crystal display drive (Select level)
V_3, V_4	2	Input	Power supply	Power supply for liquid crystal dispaly drive (Non-select level for channel 1)
V_5, V_6	2	Input	Power supply	Power supply for liquid crystal display drive (Non-select level for channel 2)
SHL1	1	Input	V_{CC} or GND	Selection of channel 1 shift register in the shift direction SHL1 / DL1 / DR1 V_{CC} / OUT / IN GND / IN / OUT
SHL2	1	Input	V_{CC} or GND	Selection of channel 2 shift register in the shift direction SHL2 / DL2 / DR2 V_{CC} / OUT / IN GND / IN / OUT
DL1, DR1	2	Input/ output	Controller or HD44100H	Data input/output of channel 1 shift register
DL2, DR2	2	Input/ output	Controller or HD44100H	Data input/output of channel 2 shift register
M	1	Input	Controller	Alternated signal for liquid crystal driver output
CL1	1	Input	Controller	Shift signal for channel 1 (↓) *1 This is used for channel 2 when FCS is GND.
CL2	1	Input	Controller	Latch signal for channel 1 (↓) *1 This is used for channel 2 when FCS is GND.
FCS	1	Input	V_{CC} or GND	Mode select signal of channel 2. FCS signal exchanges the latch signal and the shift signal of channel 2 and inverts M for channel 2.

FCS level	Channel 2		M polarity	Purpose
	Latch signal	Shift signal		
V_{CC}	CL2 ↓	CL1 ↓	$\overline{M}$	For common drive
GND	CL1 ↑	CL2 ↑	M	For segment drive
	*1	*1		*2

*1 ↓ and ↑ indicate the latches at rise and fall times respectively.

*2 The output level relationship between channel 1 and channel 2 based on the FCS signal level is as follows:

FCS	Data	M	Output level	
			1 ($Y_1 \sim Y_{20}$)	2 ($Y_{21} \sim Y_{40}$)
V_{CC} ("1")	"1" (Select)	"1"	V_1	V_2
		"0"	V_2	V_1
	"0" (Non-select)	"1"	V_3	V_6
		"0"	V_4	V_5
GND ("0")	"1" (Select)	"1"	V_1	V_1
		"0"	V_2	V_2
	"0" (Non-select)	"1"	V_3	V_5
		"0"	V_4	V_6

"1" and "0" indicate a high and low levels, respectively.

■ APPLICATIONS

• Segment Driver

When the HD44100H is used as a segment driver, the FCS is set to GND to transfer display data in the timing shown in Fig. 2. In this case, both of channel 1 and channel 2 are shift data at the fall of CL2 and latch it at the fall of CL1. V_3 and V_5, V_4 and V_6 of power supply for liquid crystal display driver are short-circuited.

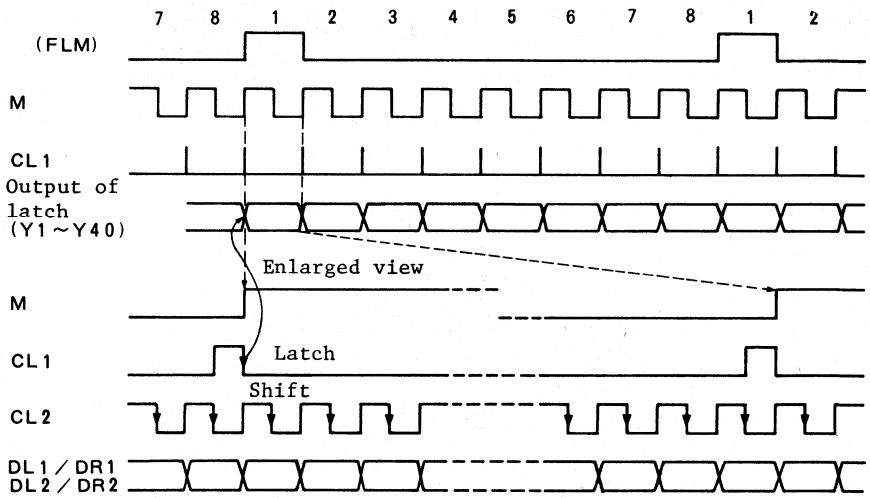


Fig. 2 Segment Data Waveforms (A type waveforms 1/8 duty)

- Common Driver

When channel 1 is used as a segment driver and channel 2 as a common driver. When channel 2 of HD44100H is used as a common driver, the FCS is set to V_{CC} level to transfer display data in the timing shown in Fig. 3. In this case, channel 2 shifts data at the rise of CL1 and latches it at the rise of CL2. Channel 1 has the same data as Fig. 2.

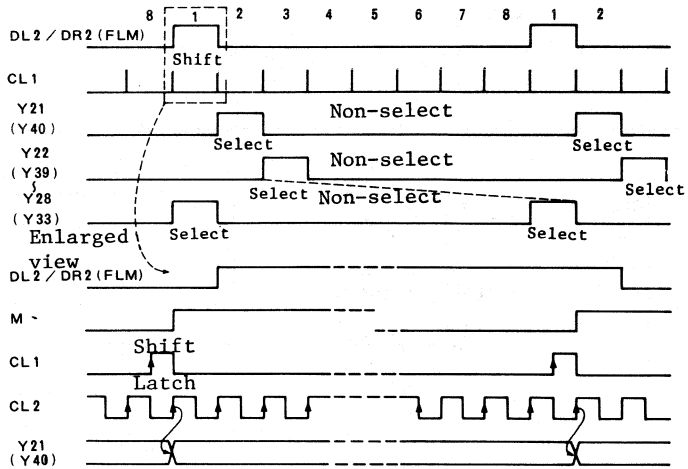


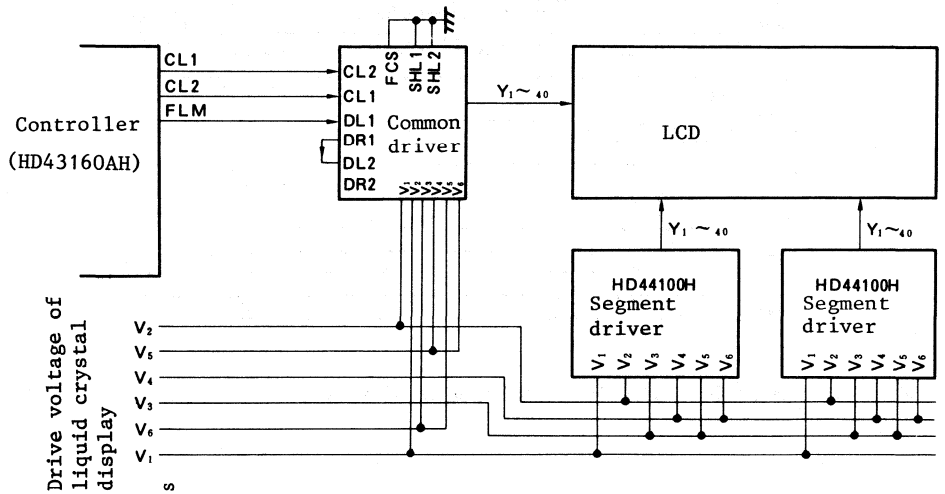
Fig. 3 Common Data Waveforms (A type waveforms of channel 2, 1/8 duty)

● When both Channel 1 and Channel 2 used as Common Drivers (FCS = GND)

When both of channel 1 and channel 2 of HD44100H are used a common driver, the FCS is set to GND and the signals (CL1, CL2, FLM) from the controller are connected to shown in following figure.

In this case, connection of power supply for liquid crystal display driver is different from segment driver, so refer to following figure.

V_1, V_2 ..... Select level of segment and common
V_3, V_4 ..... Non-select level of segment
V_5, V_6 ..... Non-select level of common



● Static Drive

When the HD44100H is used in the static drive, data is transferred at the fall of CL2 and latched at the fall of CL1. The frequency of CL1 becomes the frame frequency of liquid crystal display driver. The signal that has the frequency twice that of CL1 synchronized at the fall of CL1 is input into terminal M. The power supply for liquid crystal display driver is used by short-circuiting V_1, V_4 and V_6, and V_2, V_3 and V_5.

One of liquid crystal display driver output terminals can be used for a common output. In this case, the FCS is set to GND and data is transferred so that "0" can be always latched in the latch corresponding to the liquid crystal display driver output terminal used as the common output. If the latch signal corresponding to the segment output is "1", the segments of LCD light. They also light with common side = "1", and segment side "0".

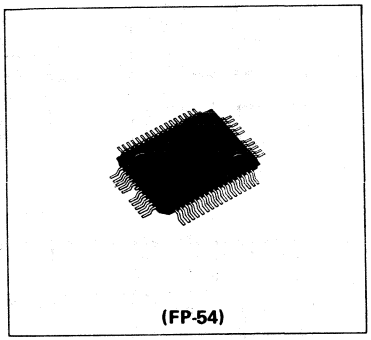
HD43160AH (CONTROLLER WITH BUILT-IN CHARACTER GENERATOR)

DISPLAY CONTROLLER AND CHARACTER GENERATOR
FOR DOT MATRIX LIQUID CRYSTAL DISPLAY SYSTEM

The HD43160AH receives character data written in the ASCII code or JIS code from microcomputer and stores them in its RAM which has 80 words capacity.

The HD43160AH converts these data into serial character pattern, then transfers them to LCD drivers.

It also generates other signals for LCD.



(FP-54)

■ CHARACTER DISPLAY

- Alphanumeric character; A ~ Z, a ~ z, @, #, %, &, etc.
- Japanese Character (katakana)
- 160 characters by internal character generator (ROM).
  (Max 256 characters by external ROM)

■ NUMBER OF CHARACTERS

- 4, 8, 16, 24, 32, 40, 64 or 80 characters in 1 or 2 lines

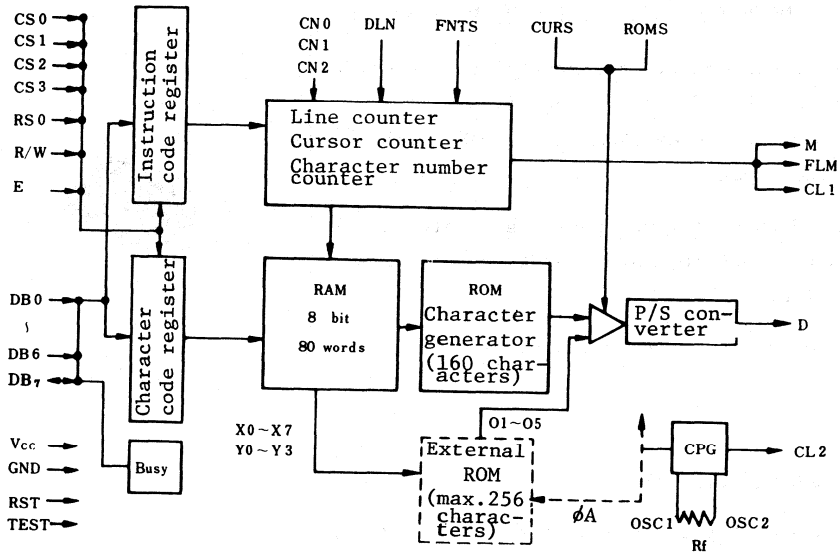
■ FRONT

- 5 × 7 + Cursor or 5 × 11 + Cursor

■ OTHER FUNCTION CONTROLLED BY MICROCOMPUTER

- Display clear
- Cursor ON/OFF
- Cursor position preset (Character position)
- Cursor return

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_T	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-40 to +125	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V±5%, GND=0V, Ta=-20 to +75°C)

Item	Symbol	Terminal No.	Test condition	min	typ	max	Unit
Input voltage (TTL compatible)	V_{IH}	CS0 ~ CS3, E, R/W,		2.0	-	V_{CC}	V
	V_{IL}	DB0 ~ DB7, RS0		0	-	0.8	V
Input voltage	V_{IHC}	OSC1, TEST, RST, FNTS, CURS, DLN, ROMS, CN0 ~ CN2, O_1 ~ O_5		0.7 V_{CC}	-	V_{CC}	V
	V_{ILC}			0	-	0.3 V_{CC}	V
Output voltage	V_{OH}	DB7	I_{OH}=-0.205mA	2.4	-	-	V
	V_{OL}		I_{OL}=1.6mA	-	-	0.4	V
Output voltage	V_{OHC}	FLM, M, D, CL1, CL2, X0 ~ X7, Y0 ~ Y3	I_{load}=±0.4mA	V_{CC}-1.0	-	-	V
	V_{OLC}			-	-	1.0	V
Input leak current	I_{in}	All inputs		-5	-	5	μA
Output leak current	I_{LO}	DB7		-10	-	10	μA
Operating frequency	f_{CP1}		R_f=200kΩ±2%, 5×7+Cursor	130	192	250	kHz
	f_{CP2}		R_f=130kΩ±2%, 5×11+Cursor	200	288	375	kHz
Input pull up current	I_{PL}	CS0 ~ CS3, RS0, R/W, DB0 ~ DB7	V_{in}=0V	2	10	20	μA
Power dissipation	P_T	*	Ta=25c, f_{CP}=400kHz (external clock)	-	-	10	mW

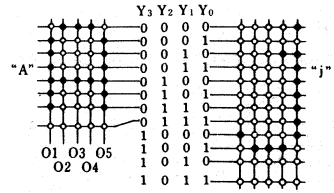
* Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low, but CS0 ~ CS3, RS0, R/W, DB0 ~ DB7 are **excluded.**

■ PIN ARRANGEMENT

Pin No.	Power sup. OSC.	Input	Output	Pin No.	Power sup. OSC.	Input	Output	Pin No.	Power sup. OSC.	Input	Output
1	GND (-)			19			D	37		DB3	
2			X4	20			FLM	38		DB4	
3			X3	21			φA	39		DB5	
4			X2	22	OSC1			40		DB6	
5			X1	23	OSC2			41		DB7	DB7
6			X0	24		RST		42		ROMS	
7		N.C.		25		TEST		43		O5	
8		N.C.		26		E		44		O4	
9		N.C.		27	V_{CC}(+)			45		O3	
10		CURS		28		R/W		46		O2	
11		FNTS		29		RS0		47		O1	
12		DLN		30		CS0		48			Y3
13		CN0		31		CS1		49			Y2
14		CN1		32		CS2		50			Y1
15		CN2		33		CS3		51			Y0
16			CL2	34		DB0		52			X7
17			CL1	35		DB1		53			X6
18			M	36		DB2		54			X5

■ PIN FUNCTION

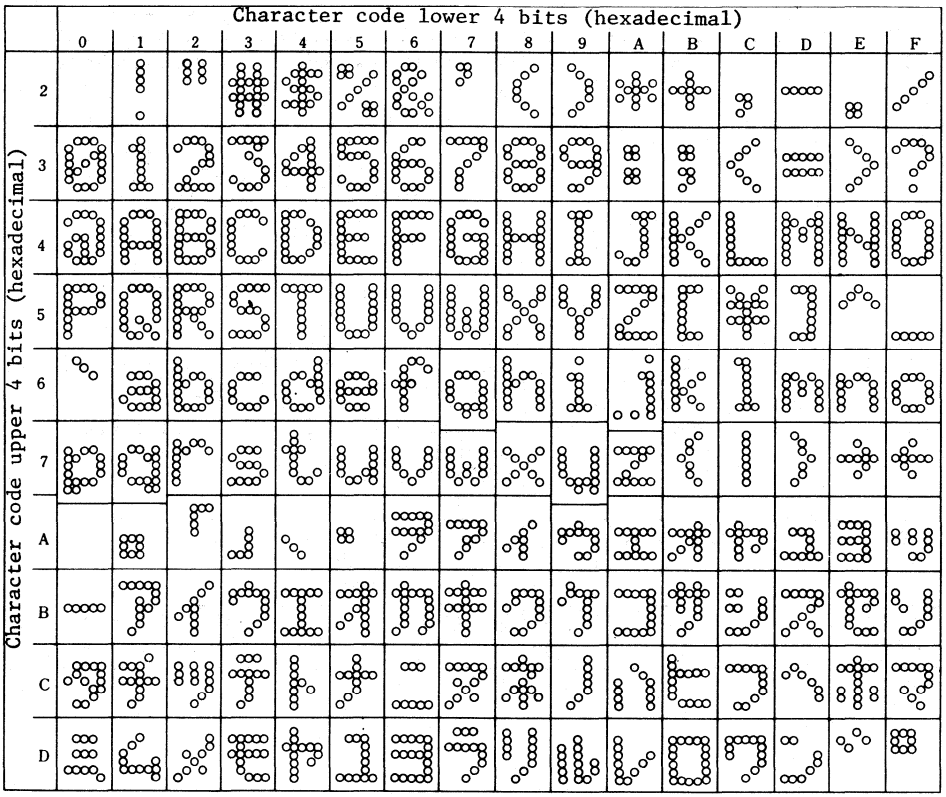
<table>
<tr><th>Pin name</th><th>Number of lines</th><th>Connected to</th><th>I/O</th><th>Function</th></tr>
<tr><td>V_{CC}
GND</td><td>2</td><td>Power supply</td><td></td><td>+5V ± 10% Power supply</td></tr>
<tr><td>CN0
CN1
CN2</td><td>3</td><td>GND or V_{CC}</td><td>I</td><td>Total displayed character number select.
<table>
<tr><th>No.</th><th>4</th><th>8</th><th>16</th><th>24</th><th>32</th><th>40</th><th>64</th><th>80</th></tr>
<tr><td>CN0</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td><td>GND</td><td>V_{CC}</td></tr>
<tr><td>CN1</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td></tr>
<tr><td>CN2</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>V_{CC}</td><td>V_{CC}</td><td>V_{CC}</td><td>V_{CC}</td></tr>
</table></td></tr>
<tr><td>CURS</td><td>1</td><td>GND or V_{CC}</td><td>I</td><td>Cursor select
V_{CC}: 5 dots. ●●●●●
GND: 1 dot. ●</td></tr>
<tr><td>DLN</td><td>1</td><td>GND or V_{CC}</td><td>I</td><td>Display line number select.
V_{CC}: 2 lines.
GND: 1 line.</td></tr>
<tr><td>FNTS</td><td>1</td><td>GND or V_{CC}</td><td>I</td><td>Font select.
V_{CC}: 5 ×11 + Cursor.
GND: 5 ×7 + Cursor.</td></tr>
<tr><td>RST</td><td>1</td><td>V_{CC}</td><td>I</td><td>Only for test. Normally V_{CC}</td></tr>
<tr><td>TEST</td><td>1</td><td>GND</td><td>I</td><td>Only for test. Normally GND</td></tr>
<tr><td>E</td><td>1</td><td>MPU</td><td>I</td><td>Strobe signal.
Write mode: The HD43160AH latches the data on DB0 ~ DB7 at the falling edge of this signal.
Read mode: Busy/Ready signal is active on DB7 while this signal is 'H'.</td></tr>
<tr><td>R/W</td><td>1</td><td>MPU</td><td>I</td><td>Read/Write signal
L: HD43160AH gets the data from MPU.
H: MPU gets the Busy/Ready signal from HD43160AH.</td></tr>
<tr><td>CS0
CS1
CS2
CS3</td><td>4</td><td>MPU</td><td>I</td><td>Chip select
When all of CS0 ~ CS3 are 'H', HD43160AH is selected.</td></tr>
<tr><td>RS0</td><td>1</td><td>MPU</td><td>I</td><td>Register select.
HD43160AH has 2 registers. One is for Character code and another is for instruction code. Each register latches the data on DB0 ~ DB7 at the falling edge of 'E', when CS0 ~ CS3 are 'H' and R/W is 'L'.
H; Character code register is selected.
L; Instruction code register is selected.</td></tr>
<tr><td>DB0
~
DB7</td><td>8</td><td>MPU</td><td>I
I/O
(DB7)</td><td>Data bus.
Inputs for Character code and Instruction code from MPU.
Output for Busy/Ready flag (DB7).</td></tr>
<tr><td>D</td><td>1</td><td>HD44100H</td><td>O</td><td>Serial dot data of characters for LCD drivers</td></tr>
<tr><td>CL2</td><td>1</td><td>HD44100H</td><td>O</td><td>Dot data shift signal for LCD drivers.</td></tr>
<tr><td>CL1</td><td>1</td><td>HD44100H</td><td>O</td><td>Dot data latch signal for LCD drivers.</td></tr>
</table>

M	1	HD44100H	O	Alternate signal for LCD drivers.
FLM	1	HD44100H	O	Signal for common plates scanning.
XO ~ X7	8	ROM	O	Character code outputs for External character generator. (for Ext ROM) X7: MSB XO: LSB ex: character 'A' MSB 0 1 0 0 0 0 0 LSB 1 '1'='H' '0'='L'
YO Y1 Y2 Y3	4	ROM	O	Character row code for External character generator. 5 ×7 + Cursor 5 ×11 + Cursor 
ϕA	1	ROM	O	Clock signal for External character generator (dynamic ROM etc.) if necessary.
O1 ~ O5	5	ROM	I	Dot data inputs from External character generator. 1(H): ON 0(L): OFF
ROMS	1	GND or V_{CC}	I	Select Internal or External ROM. H: External ROM L: Internal ROM
OSC1 OSC2	2		(I) (O)	Oscillator. 5 ×7 + Cursor : R_f=200kΩ (typ) 5 ×11 + Cursor: R_f=130kΩ (typ)

■ CHARACTER DOT PATTERNS

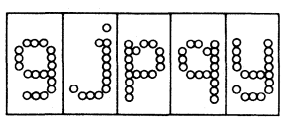
- 5 × 7

The bottom lines of the English small characters "g, i, p, q, y," are on the cursor line.



- 5 × 11

Only English small character "g, j, p, q, y," are displayed as below, the others are in the same way as that of 5 × 7.



- Cursor 5 dots: ●●●●●

  1 dot : ●

The cursor is displayed on the 8th or 12th line.

■ APPLICATION

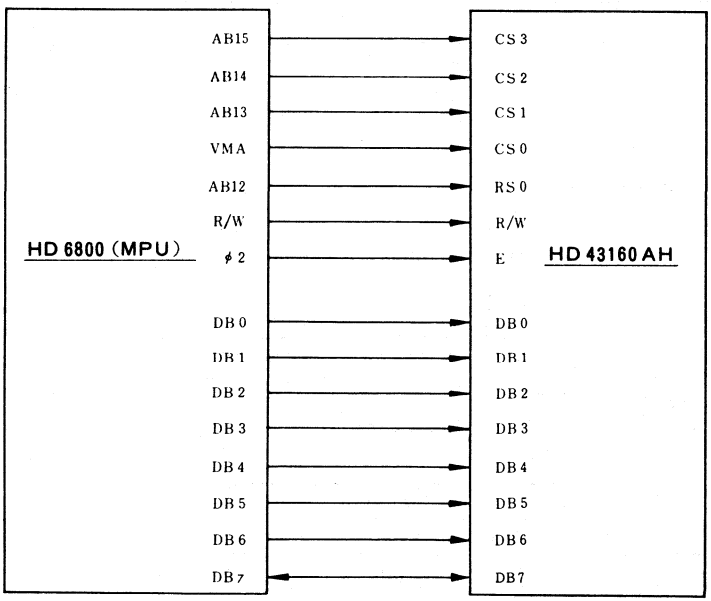
- Setting Up

  a) Total character number ..... (CN0 ~ CN2)
  b) Cursor pattern ..... (CURS)
  c) Display line number ..... (DLN)
  d) Font ..... (FNTS)

  These terminals should be connected to V_{CC} or GND according to the LCD display system. RST and TEST should be connected to V_{CC} and GND respectively.

- Interface to the Controller

  a) Example 1 Interface to HD6800

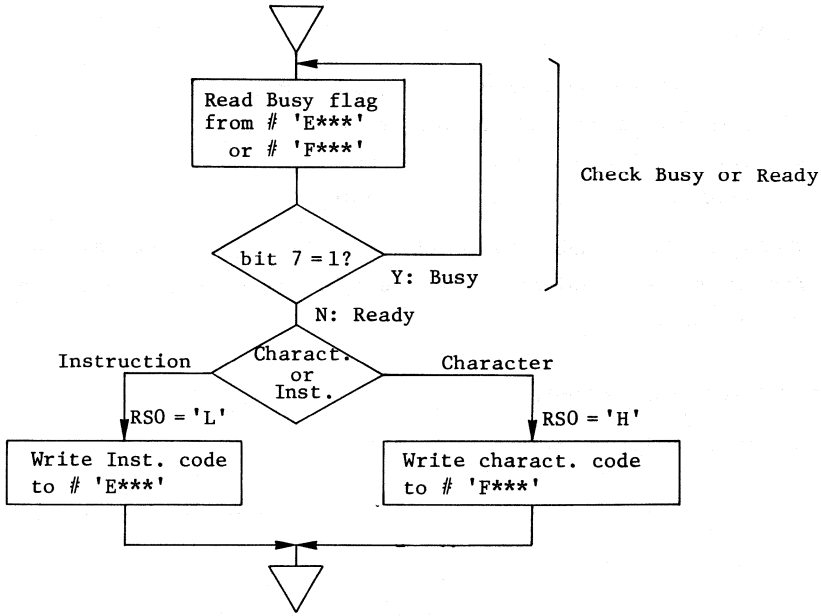


In this example, the addresses of HD43160AH in the address area of the HD6800 microcomputer are

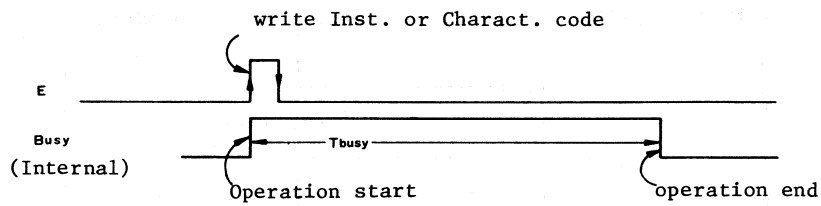
Instruction code register	#'E***'	(R/W=0)
Character code register	#'F***'	(R/W=0)
Busy flag	#'E***' or #'F***'	(R/W=1).

*: don't care
#'': hexadecimal

b) Example of display program



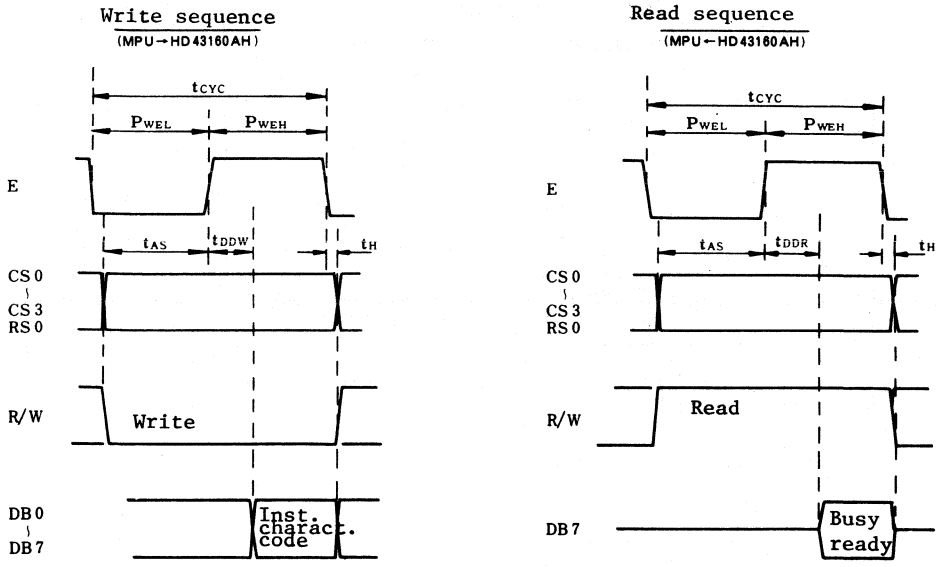
c) Time length of Busy



	T busy		
	MIN	MAX	
Display clear	$\frac{400}{Fcp}$	$\frac{410}{Fcp}$	sec
Other function	$\frac{10}{Fcp}$	$\frac{20}{Fcp}$	sec

HD43160AH begins the operation from the rising edge of 'E'. Instruction code register and Character code register latch the data on DB0 ~ DB7 at the falling edge of 'E'.

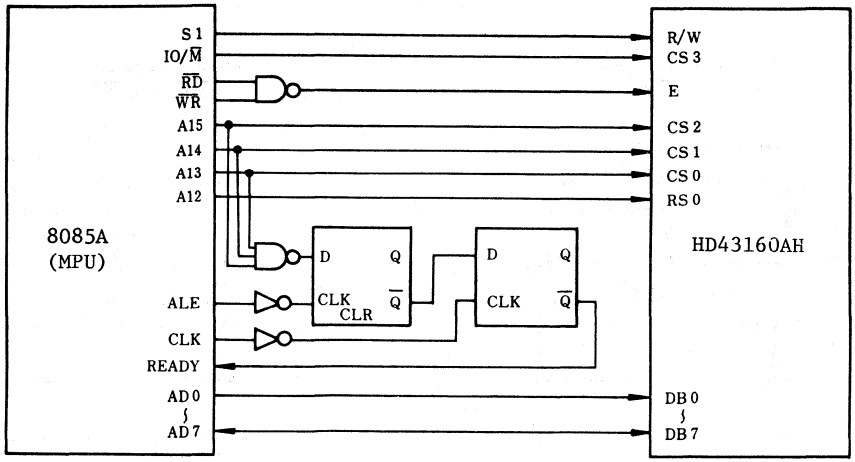
d) Timing chart



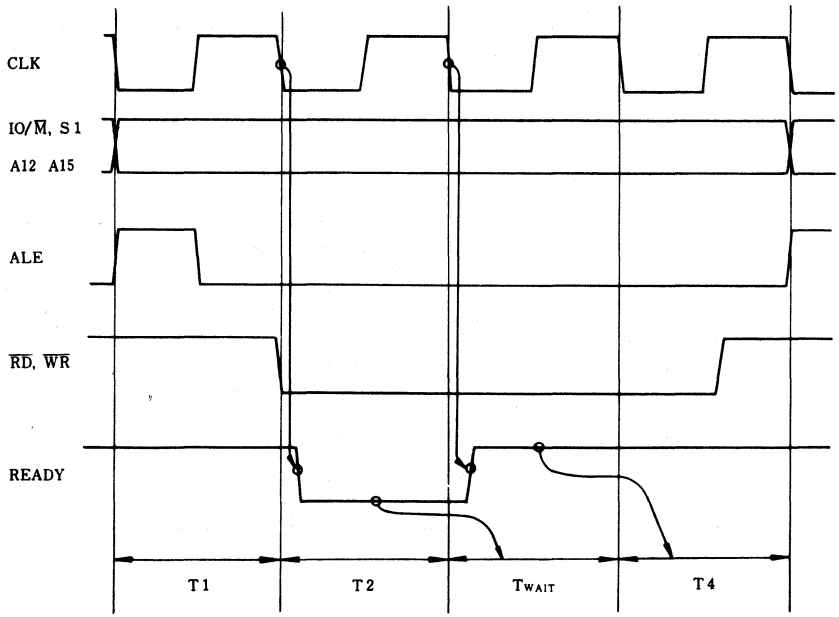
e) Timing characteristics

		Symbol	min	typ	max	Unit
Cycle time of 'E'		t_{cyc}	1.0	-	-	µs
Pulse width of 'E'	H level	P_{WEH}	0.45	-	25	µs
	L level	P_{WEL}	0.45	-	-	µs
Set up time of CS	Write	t_{AS}	140	-	-	ns
Deta delay time	Write	t_{DDW}	-	-	225	ns
	Read	t_{DDR}	-	-	300	ns
Hold time		t_H	10	-	-	ns

f) Example 2 Interface to 8085A (Intel)



g) Timing chart



Pulse widths of $\overline{RD}$ and $\overline{WR}$ signals of the 8085A are 400ns MIN, while the pulse width of E signal of the HD43160AH is 450 ns min. Therefore, in this example, $\overline{RD}$ and $\overline{WR}$ signal pulse widths are widened by using T_{WAIT} cycle.

■ DISPLAY COMMANDS

● Display Controll Instructions

These instructions should be written into the instruction register of HD43160AH by the controller. (RS0='L', R/W='L')

a) Display clear

	MSB							LSB
Code:	0	0	0	0	0	0	0	1

Operation: The screen is cleared and the cursor returns to the 1st digit.

b) Cursor return

	MSB							LSB
Code:	0	0	0	0	0	0	1	0

Operation: The cursor returns to the 1st digit and the characters being displayed do not change.

c) Cursor ON/OFF

	MSB							LSB	
Code:	0	0	0	0	0	1	0	0	(ON)
	0	0	0	0	0	1	0	1	(OFF)

Operation: The cursor appears (ON) or disappears (OFF).

d) Set cursor position

			MSB		LSB
Code:	1 line		1	(N-1) binary	
	2 lines	upper	1	0	(n-1) binary
		lower	1	1	(m-1) binary

N,n,m: digit number

Operation: The cursor moves to the Nth (nth, mth) digit.

N ≦ the total character number;

n,m ≦ 1/2 total character number.

ex 1 *1 line*

Set the cursor at 55 digit. The code is '10110110'.

ex 2 *2 lines*

Set the cursor at 35 digit of upper or lower line.

The code is '10100010' (upper).

'11100010' (lower),

- Display Character Command

When the character code is written into the character register of HD43160AH, the character of this code appears where the cursor was displayed and the cursor moves to the next digit. (RS0='H', R/W='L')

MSB LSB

code: (CHARACTER CODE)

ex 1

before ABCD_

after ABCDE_

- Read Busy Flag

When CS0 ~ CS3='H', R/W='H' and E='H' (RS0='don't care'), the Busy/Ready signal appears on DB7.

DB7 'H': BUSY

'L': READY

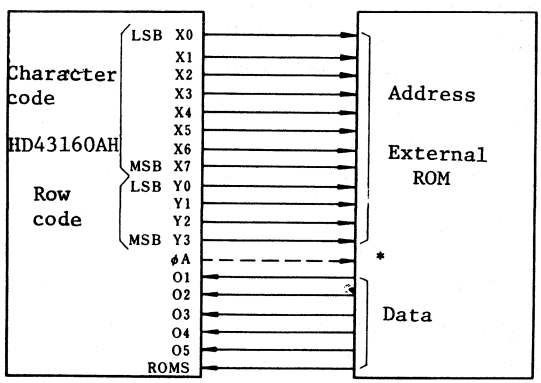
Time Length of Busy (@OSC=200kHz)

	MIN	MAX	
Display clear	2.0	2.05	ms
Other operations	50	100	µs

(depends on the operating frequency)

- Interface to External ROM

a) Example

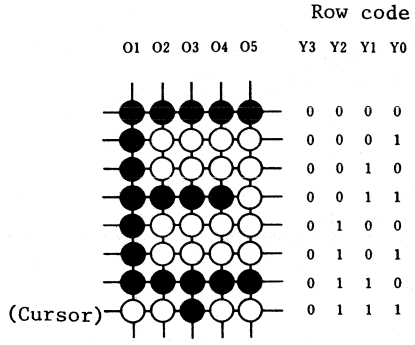


ROMS
1: Ext.
0: Int.

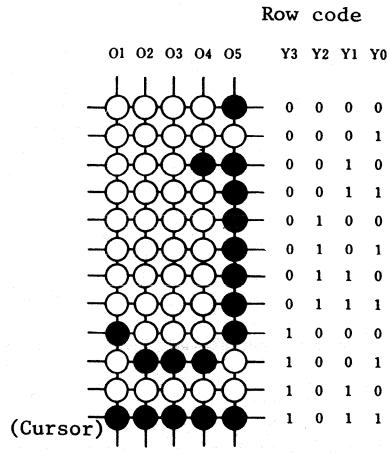
*φA is used as the precharge signal for Dynamic ROM if necessary.

Interface to External ROM

b) Row code

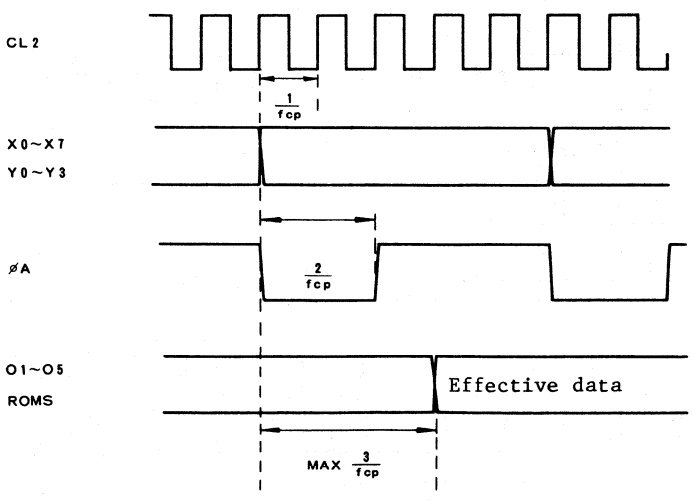


5 × 7 + Cursor



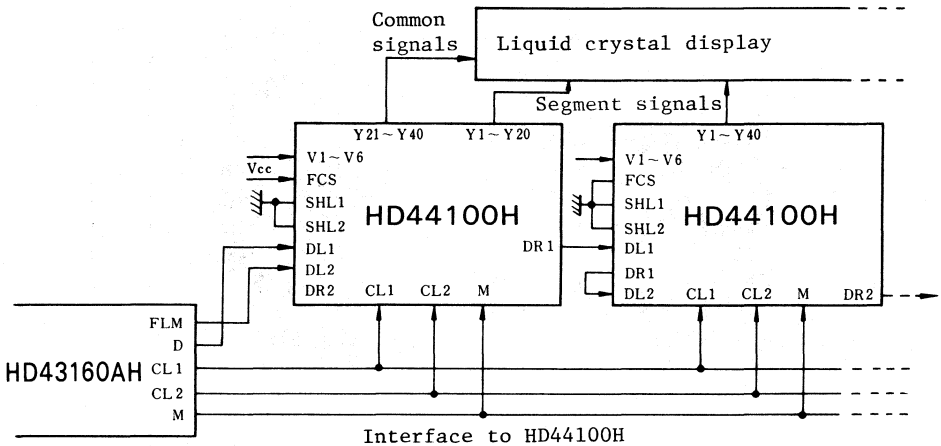
5 × 11 + Cursor

c) Timing chart



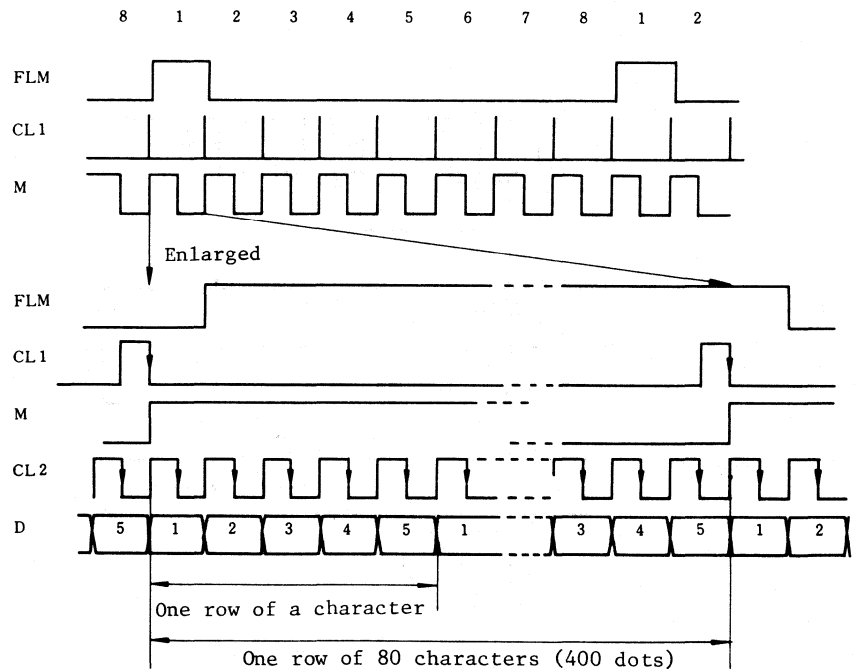
● Interface to LCD Drivers

a) Example



Interface to HD44100H

b) Wave forms (5 × 7 + Cursor 1 line)

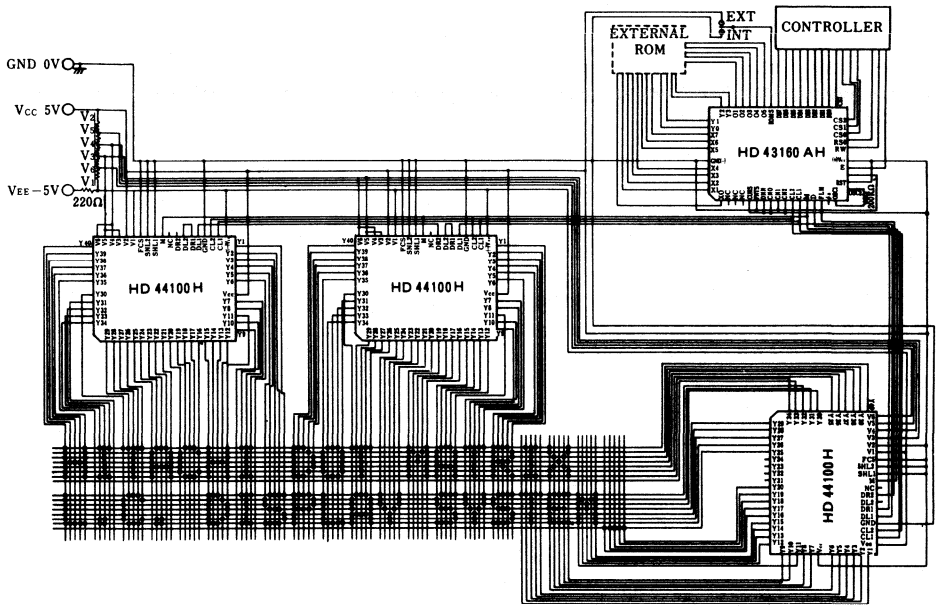


■ DOT MATRIX LIQUID CRYSTAL DISPLAY SYSTEM

Typical Application

5 ×7 + Cursor

2 Lines 40 Characters



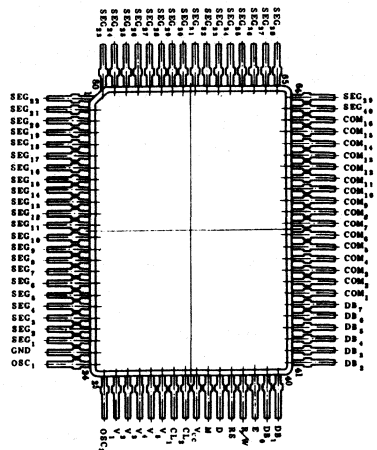
HD44780 (LCD-II) (DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER & DRIVER)

(FP-80)

The LCD-II (HD44780) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip. The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

- 5 ×7 and 5 ×10 dot matrix liquid crystal display controller driver
- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM ... 80 ×8 bits
  (80 characters, max.)
- Character generator ROM ...
  Character font 5 ×7 dots: 160 characters
  Character font 5 ×10 dobts: 32 characters

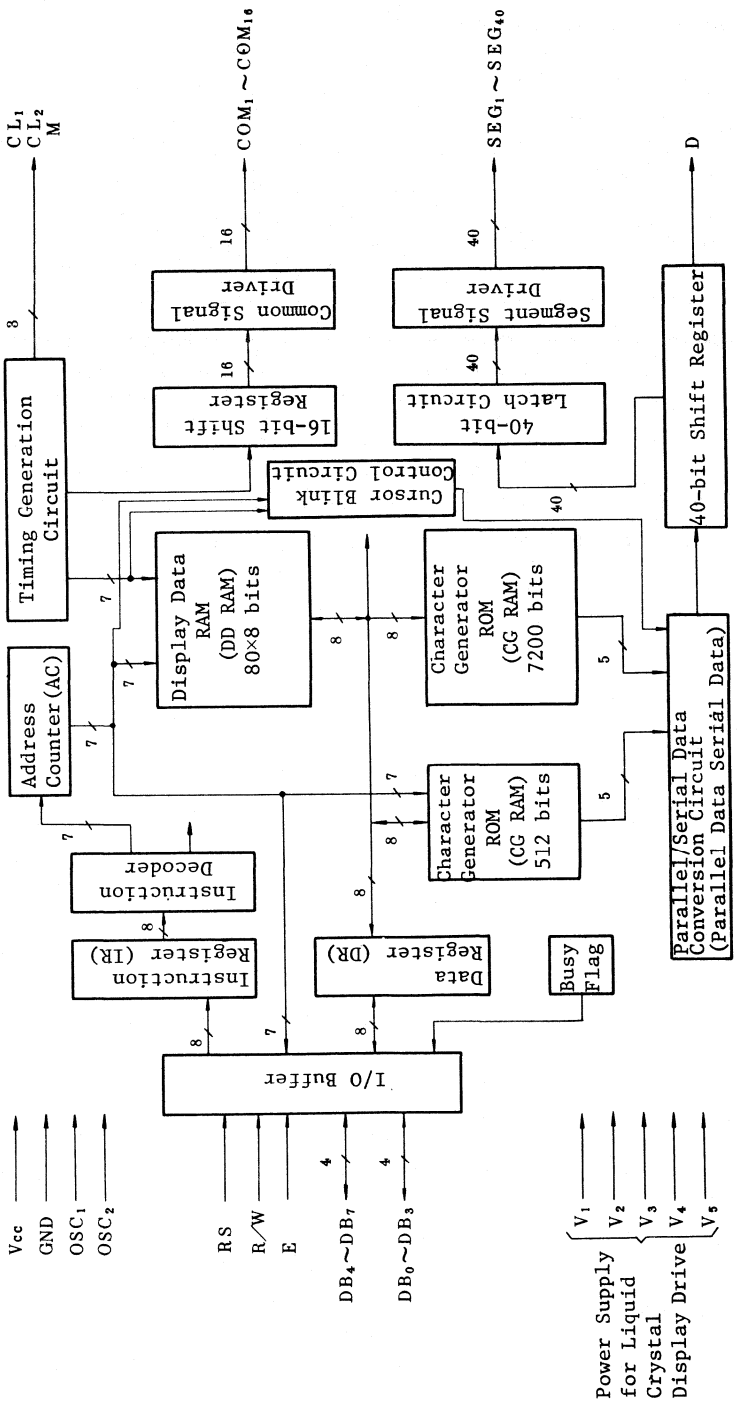
- Both display data and character generator RAMs can be read from the MPU.
- Internal liquid crystal display driver .....
  16 common signal drivers
  14 segment signal drivers (Can be externally extended to 360 segments by liquid crystal display driver HD44100H)
- Duty factor selection (selected by program) .....
  1/8 duty: 1 line of 5 × 7 dots + cursor
  1/11 duty: 1 line of 5 × 10 dots + cursor
  1/16 duty: 2 lines of 5 × 7 dots + cursor

Maximum number of display characters

No. of display lines	Duty factory	Extension	HD44780	HD44100H	No. of display characters
1-line display	1/8 1/11 duty	Not provided	1 pc.	—	8 characters ×1 line
		provided	1 pc.	9 pcs. (8 characters/pc.)	80 characters ×1 line
2-line display	1/16 duty	Not provided	1 pc.	—	8 characters ×2 lines
		provided	1 pc.	4 pcs.(8 characters ×2 lines/pc)	40 characters ×2 lines

- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF,
  Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)
- Internal oscillation circuit (with external resistor or ceramic filter)
  (External clock operation possible)
- CMOS process
- Logic power supply: A single + 5V (excluding power for liquid crystal display drive)
- Operation temperature range: -20 ~ +75°C
  (Device for -40 ~ +85°C available upon request)
- 80-pin plastic flat package (FP-80)

■ BLOCK DIAGRAM (HD44780 INTERIOR)



■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}-13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	-0.3 to V_{CC}+0.3	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-55 to +125	°C	

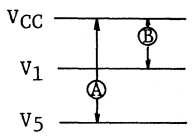
Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND=0V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$

(high ← → low)

● Electrical Characteristics (V_{CC} = 5V±10%, Ta = -20 to +75°C)



Ⓐ = V_{CC}-V_5
Ⓑ = V_{CC}-V_1
Ⓐ ≧ 1.5V
Ⓑ ≦ 0.25 ×A

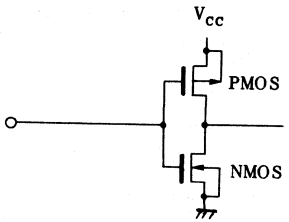
The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	V_{CC}	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
Output "High" Voltage (1)(TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA	-	-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	0.9V_{CC}	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	L_{OL}=0.04mA	-	-	0.1V_{CC}	V	(4)
Driver Voltage Descending (COM)	V_{COM}	Id=0.05mA	-	-	2.9	V	(10)
Driver Voltage Descending (SEG)	V_{SEG}	Id=0.05mA	-	-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	µA	(5)
Pull up MOS Current	$-I_p$	V_{CC}=5V	50	125	250	µA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}= 250kHz	-	0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}= fcp=270kHz	-	0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	250	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}		-	-	0.2	µs	(7)
External Clock Fall Time	t_{fcp}		-	-	0.2	µs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	V_{CC}	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-0.3	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage	V_{LCD1}	V_{CC}-V_5 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	V_{CC}-V_5 1/4 bias	3.0	-	11	V	(13)

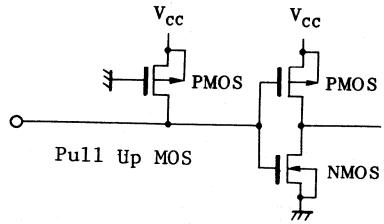
Note 1: The following are I/O terminal configurations except for liquid crystal display output.

- Input Terminal

Applicable Terminals: E
(No pull up MOS)

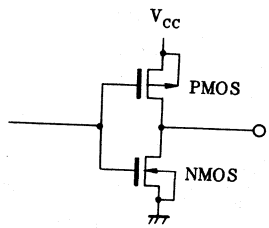


Applicable Terminals: RS, R/W
(With pull up MOS)



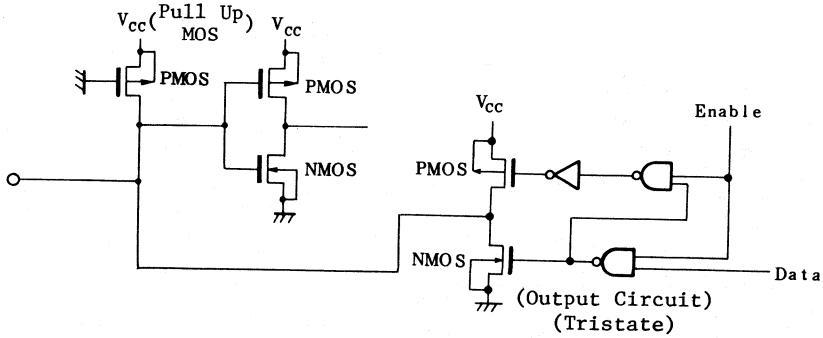
- Output Terminal

Applicable Terminals: CL_1, CL_2, M, D



- I/O Terminal

Applicable Terminals: DB_0 to DB_7



Note 2: Input terminals and I/O terminals. Excludes OSC_1 terminals.

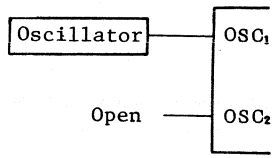
Note 3: I/O terminals.

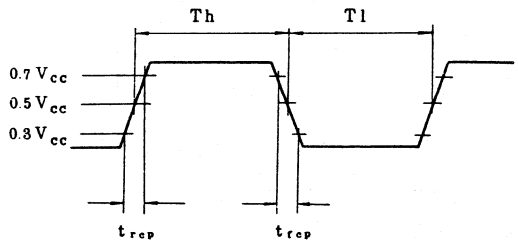
Note 4: Output terminals.

Note 5: Current flowing through pull-up MOS's and output drive MOS's is excluded.

Note 6: Input/Output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

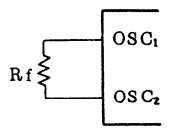
Note 7: External clock operation.





$$Duty = \frac{Th}{Th + Tl} \times 100\%$$

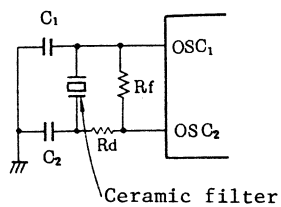
Note 8: Internal oscillator operation using oscillation resistor Rf.



Rf : 91kΩ± 2 %

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length for these terminals should be minimized.

Note 9: Internal oscillator operation using a ceramic filter.is used.



Ceramic filter: CSB250A (Murata)

Rf: 1MΩ ±10%

C_1: 680pF±10%

C_2: 680pF±10%

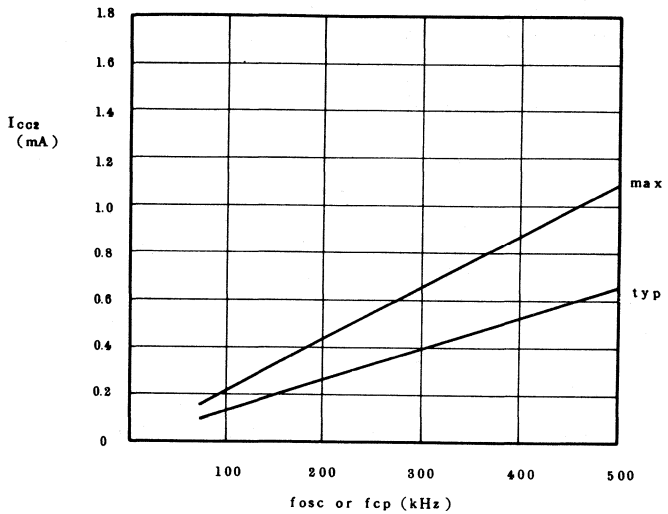
Rd: 3.3kΩ±5%

Note 10: Applies to both V_{COM} and V_{SEG} voltage drops.

V_{COM}: From poer supply terminal V_{CC}, V_1, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})

V_{SEG}: From power supply terminal V_{CC}, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

Note 11: Relation between operation frequency and current consumption is shown in this diagram. (V_{CC} = 5V)



Note 12: Applied to OSC_1 terminal.

Note 13: The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

● Timing Characteristics

Write Operation

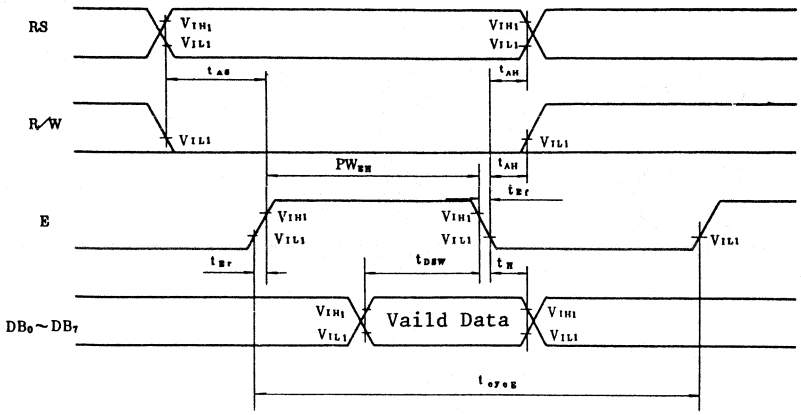


Fig. 1 Bus Write Operation Sequence
(Writing data from MPU to HD44780)

Read Operation

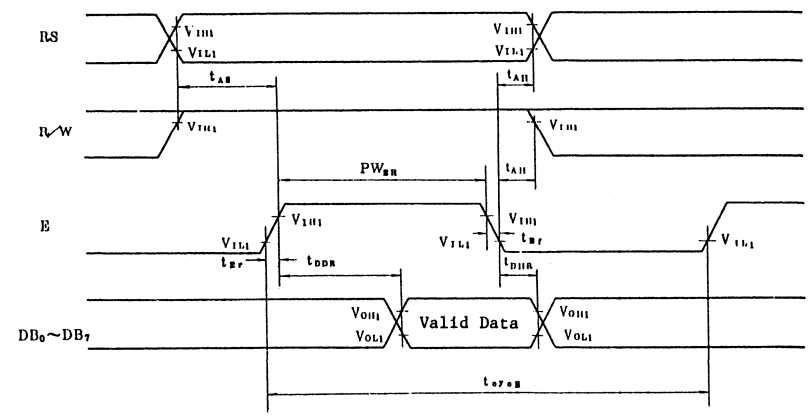


Fig. 2 Bus Read Operation Sequence
(Reading out data from HD44780 to MPU)

Interface Signal with Driver LSI HD44100H

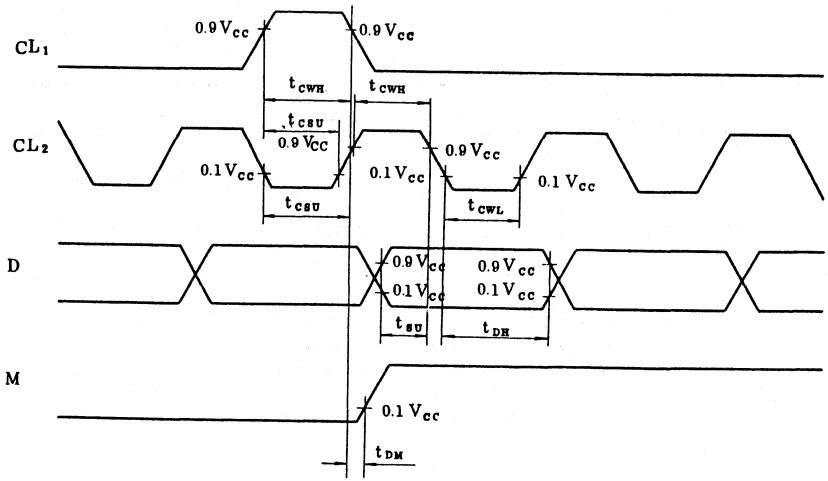


Fig. 3 Sending Data to Driver LSI HD44100H

● Bus Timing Characteristics (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

Write Operation (Writing data from MPU to HD44780)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		t_{cycE}	Fig. 1	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	450	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	140	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	195	-	ns
Data Hold Time		t_H	Fig. 1	10	-	ns

Read Operation (Reading data from HD44780 to MPU)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Enable Cycle Time		t_{cycE}	Fig. 2	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	450	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	140	-	ns
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	320	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

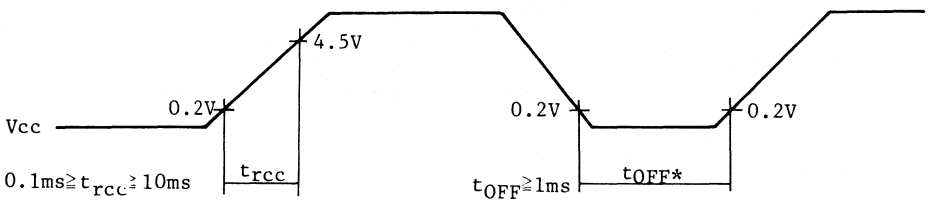
● Interface Signal with HD44100H Timing Characteristics
(V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

Item		Symbol	Test condition	Limit		Unit
				min	max	
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock Pulse Width	"High" level	t_{CWL}	Fig. 3	800	-	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	-	ns
Data Set-up Time		t_{SU}	Fig. 3	300	-	ns
Data Hold Time		t_{DH}	Fig. 3	300	-	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

● Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Test condition	Limit		Unit
			min	max	
Power Supply Rise Time	trcc	-	0.1	10	ns
Power Supply OFF Time	t_{OFF}	-	1	-	ns

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction.
(Refer to "Initializing by Instruction")



(Note) t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.

■ Terminal Function

Table 1 Functional Description of Terminals

Signal name	No. of lines	Input/ Output	Connected to	Function
RS	1	Input	MPU	Signal to select registers "0": Instruction register (for write) Busy flag; address counter (for read) "1": Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W) "0": Write "1": Read
E	1	Input	MPU	Operation start signal for data read/ write
DB_4 ~ DB_7	4	Input/ Output	MPU	Higher order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the HD44780. DB_7 can be used as a BUSY flag.
DB_0 ~ DB_3	4	Input/ Output	MPU	Lower order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the HD44780. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Character pattern data corresponding to each common signal is serially sent. "0": Non selection "1": Selection
COM_1 ~ COM_{16}	16	Output	Liquid crystal display	Common signals that are not used are charged to non-selection waveforms. That is, COM_9 ~ COM_{16} are in non-selection waveform at 1/8 duty factor, and COM_{12} ~ COM_{16} are in non-selection waveform at 1/11 duty factor.
SEG_1 ~ SEG_{40}	40	Output	Liquid crystal display	Segment signal
V_1 ~ V_5	5		Power supply	Power supply for liquid crystal display drive
V_{CC}, GND	2		Power supply	V_{CC}; +5V, GND; 0V
OSC_1, OSC_2	2			Terminals connected to resister or ceramic filter for internal clock osillation. For external clock operation, the clock is input to OSC_1.

■ FUNCTION OF EACH BLOCK

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MRU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB_7) and address counter (DB_0 ~ DB_6)
1	0	DR write as internal operation (DR to DD or CG RAM)
1	1	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 2 shows, the busy flag is output to DB_7 when RS=0 and R/W=1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

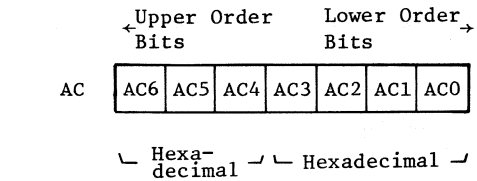
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB_0 ~ DB_6 when RS=0 and R/W=1, as shown in Table 2.

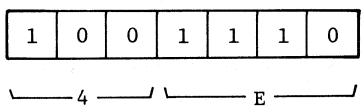
(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80×8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

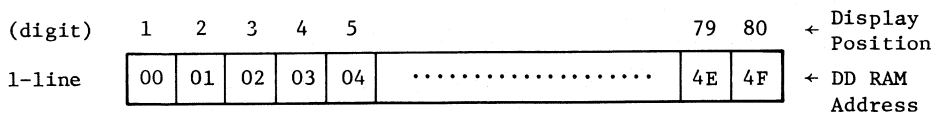
The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



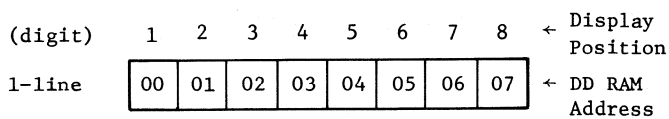
(Example) DD RAM address "4E"



1-line Display (N=0)



(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using 1 HD44780 are displayed as:



When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display)

01	02	03	04	05	06	07	08

(Right Shift Display)

4F	00	01	02	03	04	05	06

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address

└── HD44780 Display ──┘└── HD44100H Display ──┘

When the display shift operation is performed, the DD RAM address moves as:

(Left Shift Display)

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

(Right Shift Display)

4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	...	73	74	75	76	77	78	79	80	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	----	48	49	4A	4B	4C	4D	4E	4F	← DD RAM Address

└── HD44780 Diaplay ──┘└── HD44100H(1) Display ──┘└── HD44100H (2)∿(8) Display ──┘└── HD44100H(9) Display ──┘

2-line Display (N=1)

(digit)	1	2	3	4	5	...	39	40	← Display Position
1-line	00	01	02	03	04	.....	26	27	← DD RAM Address
2-line	40	41	42	43	44	.....	66	67	

(a) When the number of display characters is less than 40 × 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters × 2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display Position
1-line	00	01	02	03	04	05	06	07	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address moves as:

(Left Shift Display)	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48

(Right Shift Display)	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

(b) 16 characters × 2 lines are displayed when an HD44780 and an HD44100H are used.

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

└── HD44780 Display ──┘└── HD44100H Display ──┘

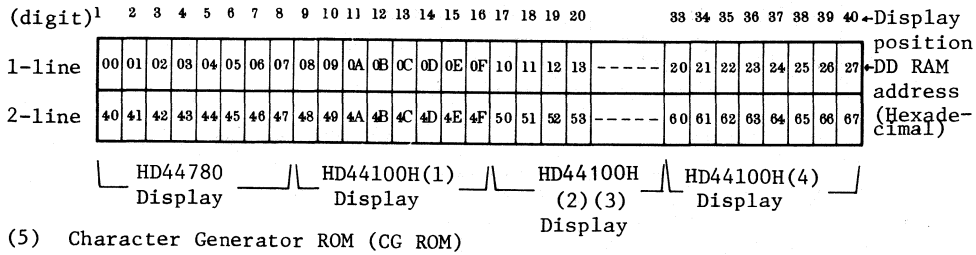
When display shift is performed, the DD RAM address moves as follows:

(Left Shift Display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Right Shift Display)	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits × 2 lines for each additional HD44100H, up to 40 digits 2 lines can be displayed by connecting 4 HD44780's externally.



(5) Character Generator ROM (CG ROM)

The character generator ROM generates 5 × 7 dot or 5 × 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 × 7 dot character patterns and 32 types of 5 × 10 dot character patterns. Table 3 and 4 show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM. For details, see "The LCD-II (HD44780) Breadboard User's Manual".

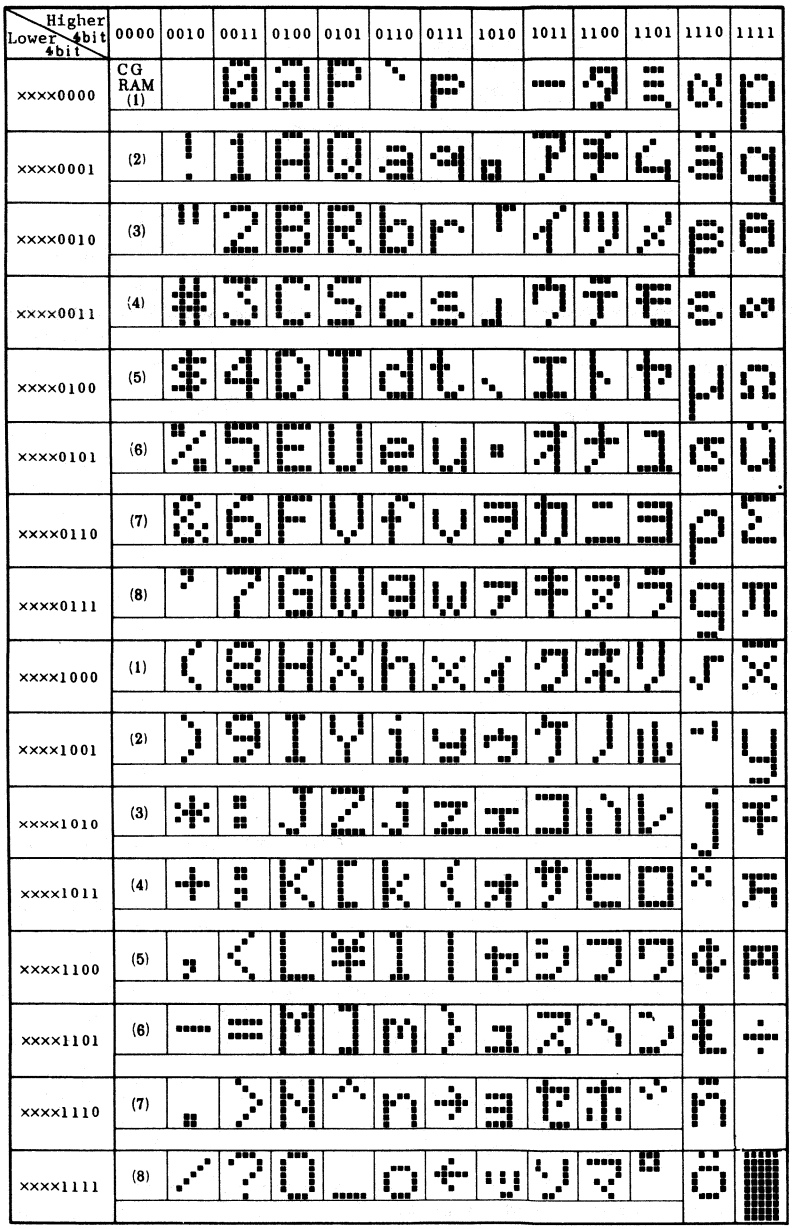
(6) Character Generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 × 7 dots, 8 byptes of character patterns can be written and with 5 × 10 dots 4 types can be written. Write the character codes in the left columns of Tables 3 and 4 to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

As Table 5 shows, an area that is not used for display can be used as a general data RAM.

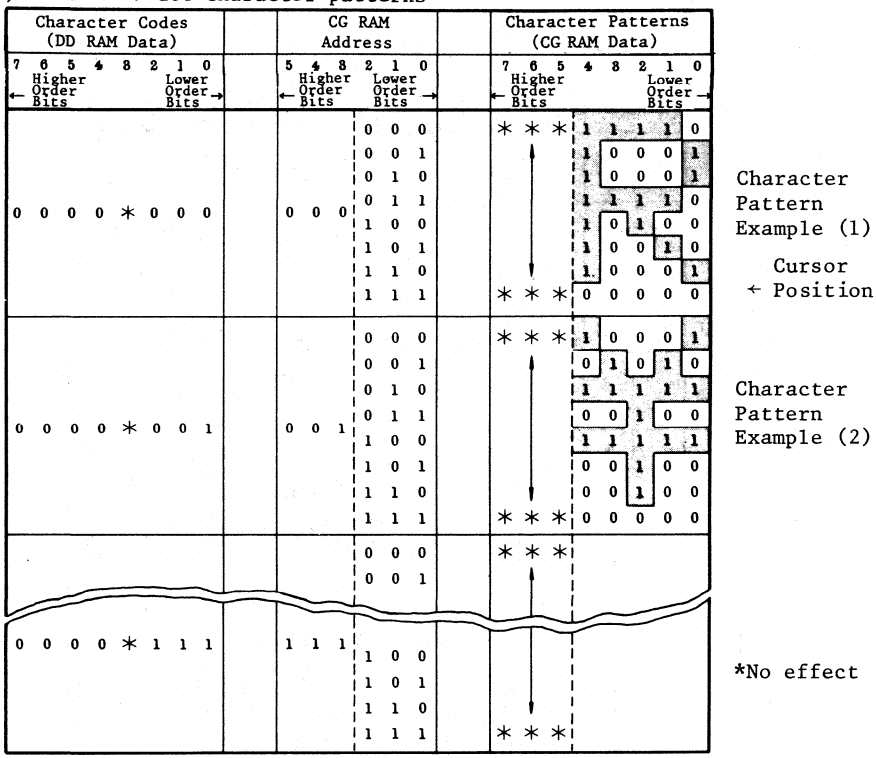
Table 3 Correspondence between Character Codes and Character Pattern
(Hitachi Standard HD44780A00)



* The user can specify any pattern for character-generator ROM.

Table 4 Relation between CG RAM Addresses and Character Codes (DD RAM) and Character Patterns (CG RAM Data)

(a) For 5 × 7 dot character patterns



(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.

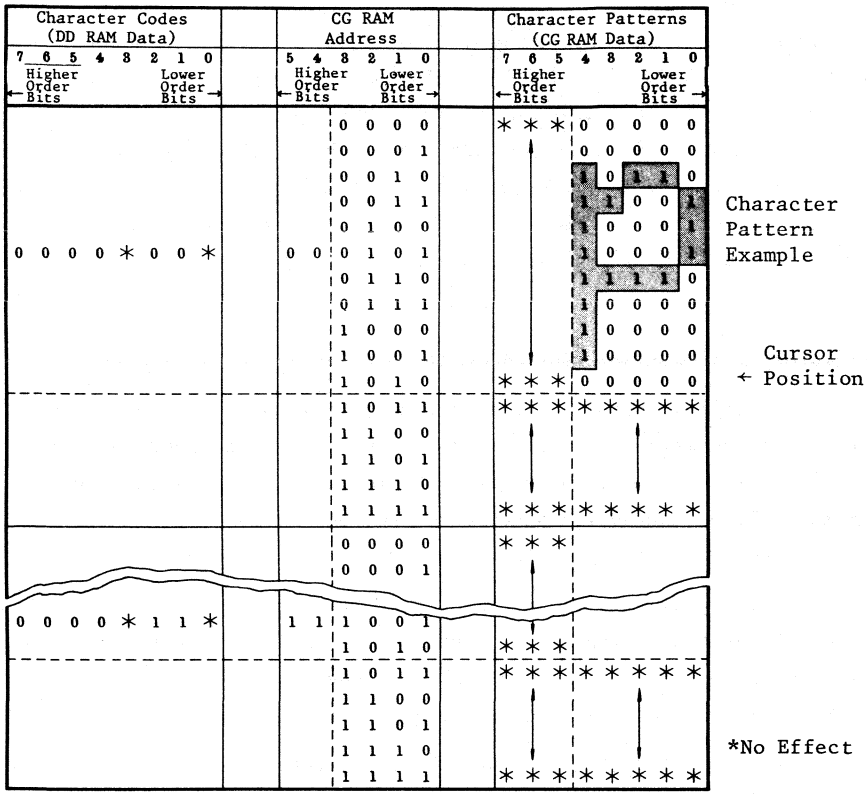
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Table 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit,the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(b) For 5 ×10 dot character patterns



(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.

Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 × 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(7) Timing Generation Circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undersirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension.

Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

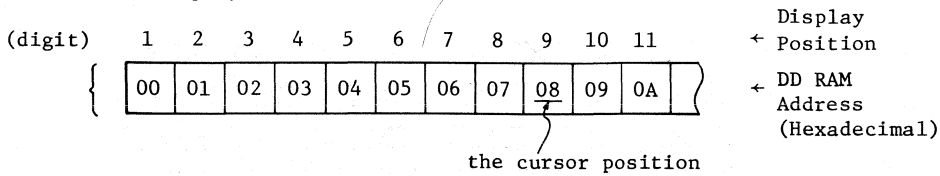
(9) Cursor/Blink Control Circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

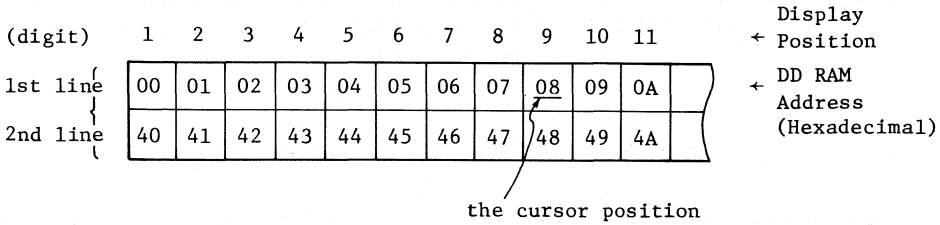
When the address counter is $(08)_{16}$, a cursor position is:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

In a 1-line display



In a 2-line display



(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.

The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

■ INTERFACING TO MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interace to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred.

Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

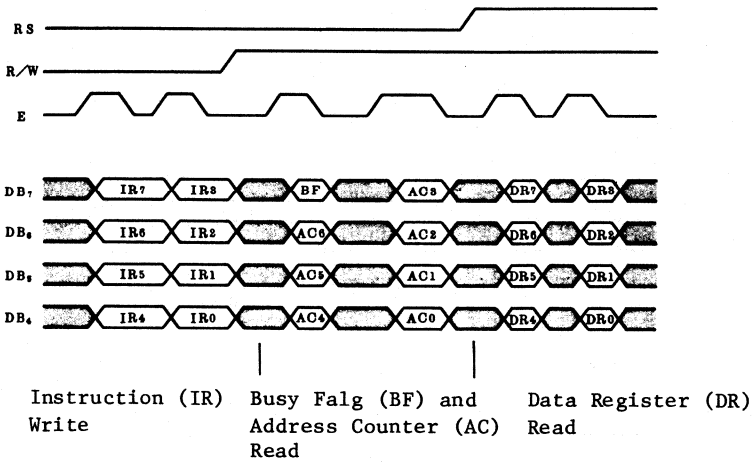


Fig. 4 4-bit Data Transfer Example

(2) When interface data is 8 bits long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

■ RESET FUNCTION

● Initializing by Internal Reset Circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10 ms after V_{CC} rises to 4.5V.

(1) Display clear

(2) Function ser ..... DL=1 : 8 bit long interface data
N =0 : 1-line display
F =0 : 5 × 7 dot character font

(3) Display ON/OFF control ..... D =0 : Display OFF
C =0 : Cursor OFF
B =0 : Blink OFF

(4) Entry mode set ..... I/D=1: +1 (increment)
S =0 : No shift

(Note) When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit with not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

■ INSTRUCTION

● Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 5 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.

(2) Give internal RAM addresses.

(3) Perform data transfer with internal RAM

(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by -1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programing efficiency. For an explanation of the shift function in its relation to display, see Table 7.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed. Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

(Note) Make sure the HD44780 is not in the busy state (BF=0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 5 for a list of each instruction execution time.

Table 5 Instructions

Instruction	Code										Description	Execution time (max) (when fcp or fosc is 250kHz)
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in adress counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40μs
Read Data from CG or DD RAM	1	0	Read Data								Reads data from DD RAM or CG RAM.	40μs
	I/D=1 : Increment I/D=0 : Decrement S =1 : Accompanies display shift. S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right. R/L=0 : Shifts to the left. DL =1 : 8 bits, DL=0 : 4 bits. N =1 : 2 lines, N=0 : 1 line F =1 : 5×10 dots, F=0 : 5×7 dots BF =1 : Internally operating BF =0 : Can accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM ACC : CG RAM address ADD : DD RAM address. Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fcp or fosc is 270kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

* No Effect

Description of Details

(1) Clear Display

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal)(character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the dispaly (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return Home

	RS	R/W	DB_7						DB_0	
Code	0	0	0	0	0	0	0	0	*	* Don't care

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry Mode Set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D=1) or decrements (I/D=0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S : Shifts the entire display either to the right or to the left when S is 1; to the left when I/D=1 and to the right when I/D=0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S=0.

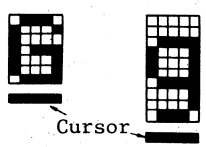
(4) Display ON/OFF Control

	RS	R/W	DB_7						DB_6
Code	0	0	0	0	0	0	1	D	C	B

D : The display is ON when D=1 and OFF when D=0. When off due to D=0, display data remains in the DD RAM. It can be displayed immediately by setting D=1.

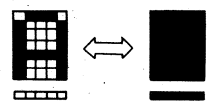
C : The cursor displays when C=1 and does not display when C=0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 × 7 dot character font is selected and 5 dots in the 11th line when the 5 × 10 dot character font is selected.

B : The character indicated by the cursor blinks when B=1. The blink is displayed by switching between all blank dots and display characters at 409.6ms interval when fcp or fosc=250kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of fcp or fosc. $409.6 \times \frac{250}{270} = 379.2$ms when fcp=270kHz.)



5 × 7 dot character font　　5 × 10 dot character font

(a) Cursor Display Example



Alternating display

(b) Blink Display Example

(5) Cursor or Display Shift

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Don't care

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line postion.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function Set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* (Don't care)

DL : Sets interface data length. Data is sent or received in 8 bit lengths (DB_7 ~ DB_0) when DL=1 and in 4 bit lengths (DB_7 ~ DB_4) when DL=0.
When the 4 bit length is selected, data must be sent or received twice.

N : Sets number of display lines.

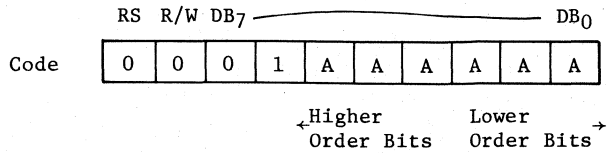
F : Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N	F	No. of display lines	Character font	Duty factor	Remarks
0	0	1	5 ×7 dots	1/8	
0	1	1	5 ×10 dots	1/11	
1	*	2	5 ×7 dots	1/16	Cannot display 2 lines with 5 ×10 dot character font.

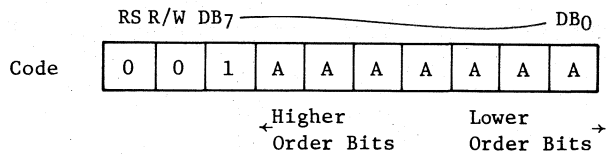
* (Don't care)

(7) Set CG RAM Address



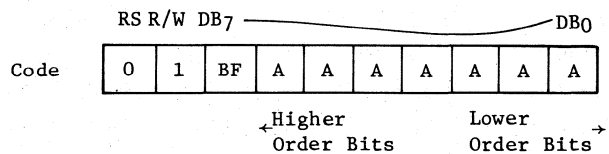
Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM Address



Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.
However, when N=0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal).
when N=1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

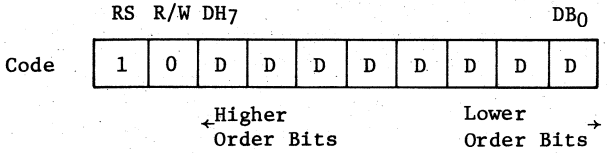
(9) Read Busy Flag and Address



Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF=1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

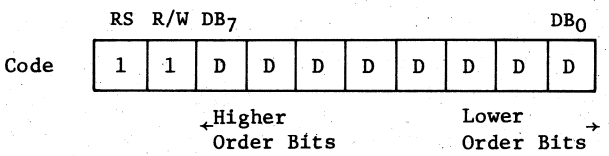
(10) Write Data to CG or DD RAM



Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM.

Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read Data from CG or DD RAM



Reads binary 8 bit data DDDDDDDD from the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift in struction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set

instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

■ HOW TO USE THE HD44780

● Interface to MPU

(1) Interface to 8-bit MPU

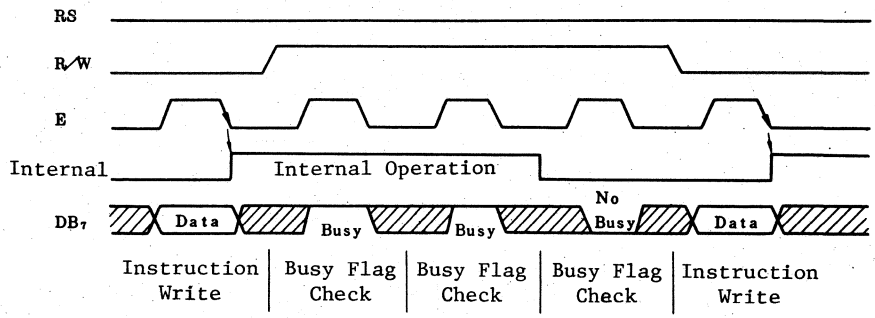
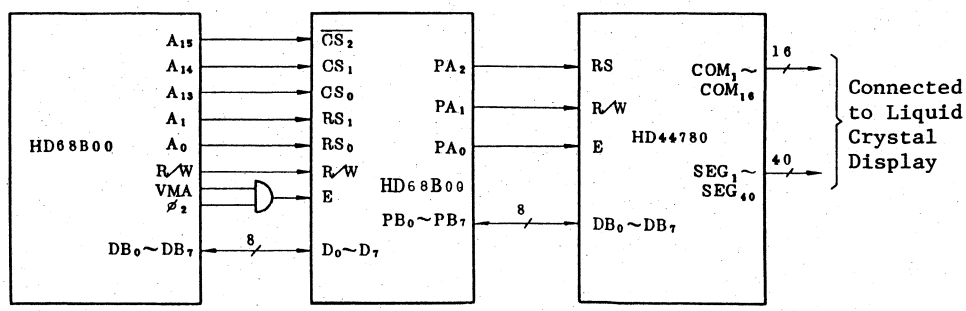


Fig. 5 Example of Busy Flag Check Timing Sequence

① When connecting to 8-bit MPU through PIA

Fig. 6-2 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

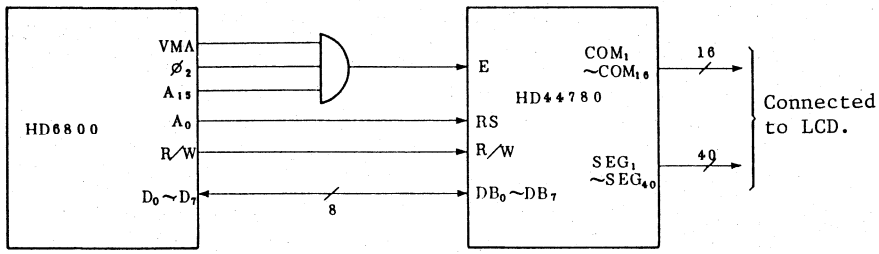
In the example, PB_0 to PB7 are connected to the data buses DB_0 to DB7 and PA0 to PA2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.



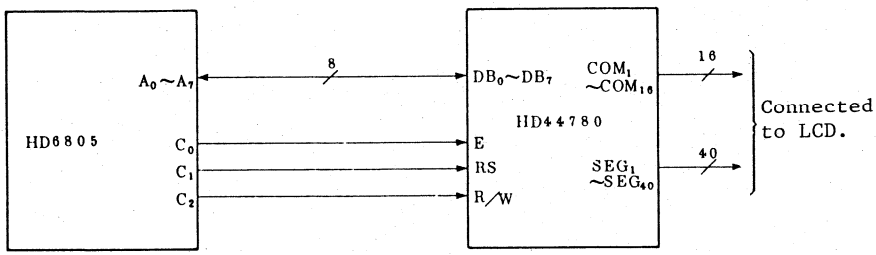
HD68B00: 8 bit CPU

Fig. 6 Example of Interface to HD68B00 Using PIA (HD68B21)

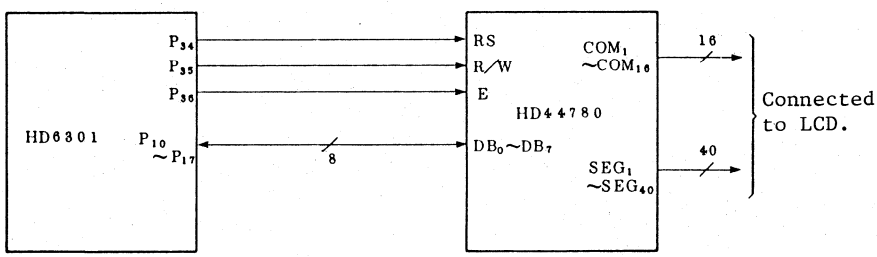
② Connecting directly to the 8-bit MPU bus line



③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301

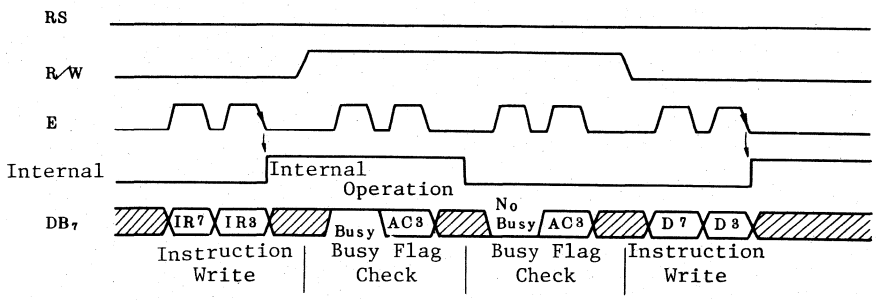


(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 7)

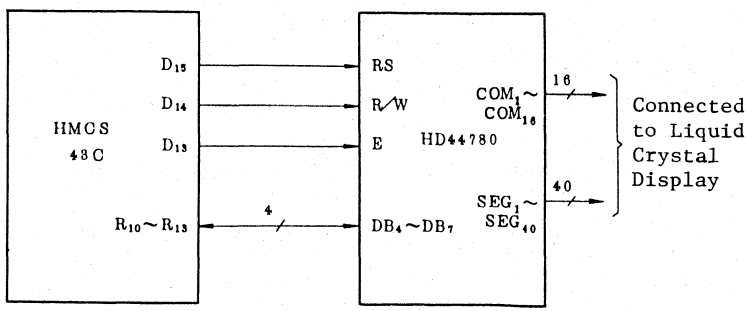
Fig. 8 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



(Note) IR7, IR3: Instruction 7th bit, 3rd bit
AC3 : Address Counter 3rd bit

Fig. 7 An Example of 4-bit Data Transfer Timing Sequence



HMCS43C: Hitachi 4-bit single-chip microcomputer

Fig. 8 Example of Interface to the HMCS43C

Interface to Liquid Crystal Display

(1) Character Font and Number of Lines

The HD44780 can perform 2 types of display, 5 ×7 dots and 5 ×10 dots as character font, with a cursor on each.

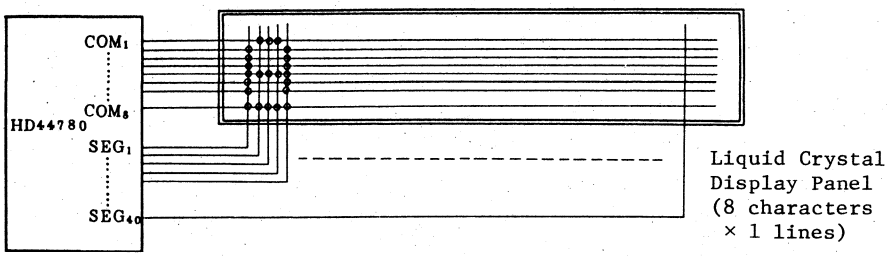
Up to 2 lines are displayed with 5 ×7 dots and 1 line with 5 ×10 dots. Therefore, three types of common signals are available:

Number of Lines	Character Font	Number of Common Signals	Duty Factor
1	5 ×7 dots + Cursor	8	1/8
1	5 ×10 dots + Cursor	11	1/11
2	5 ×7 dots + Cursor	16	1/16

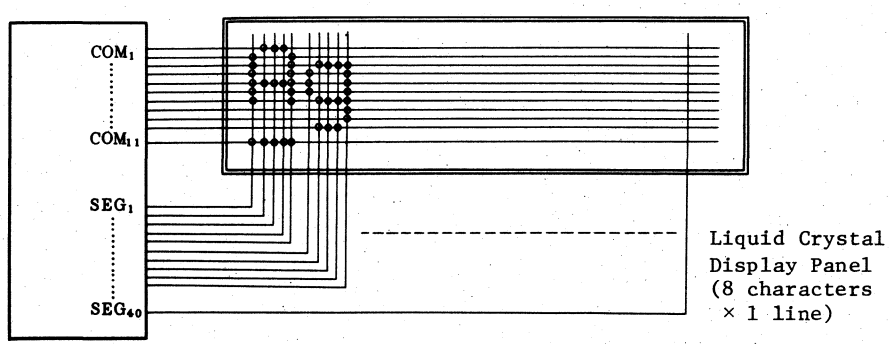
Number of lines and font types can be selected by program. (See to Table 5 Instruction)

(2) Connection to HD44780 and Liquid Crystal Display

Fig. 9 (1) and (2) show connection examples.

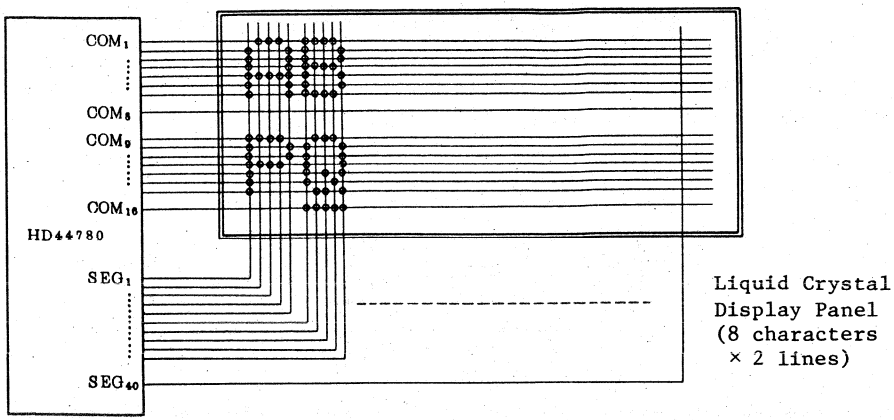


(a) Example of a 5 ×7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)



(b) Example of a 5 ×10 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

Fig. 9 (1) Liquid Crystal Display and Connections to HD44780

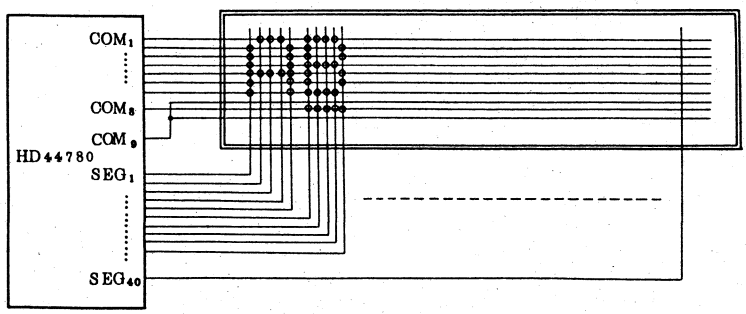


(c) Example of 5 × 7 dot, 8 character × 2 lines Display (1/5 Bias, 1/16 Duty)

Fig. 9 (2) Liquid Crystal Display and Connection to HD44780

Since 5 signal lines at the SEG can display one digit, one HD44780 can display up to 8 digits for 1-line display and 16 digits for 2-line display.

In Fig. 9 examples (a) and (b), there are unused common signal terminals, non-selection waveforms which always output. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals.

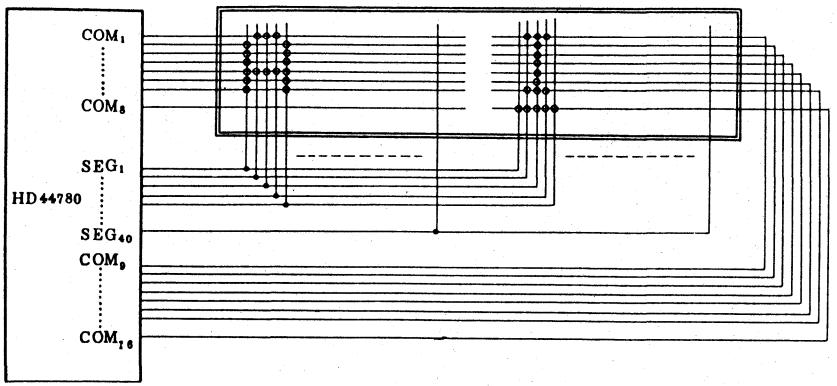


5 × 7 dot, 8 character × 1 line Display (1/4 Bias, 1/8 Duty)

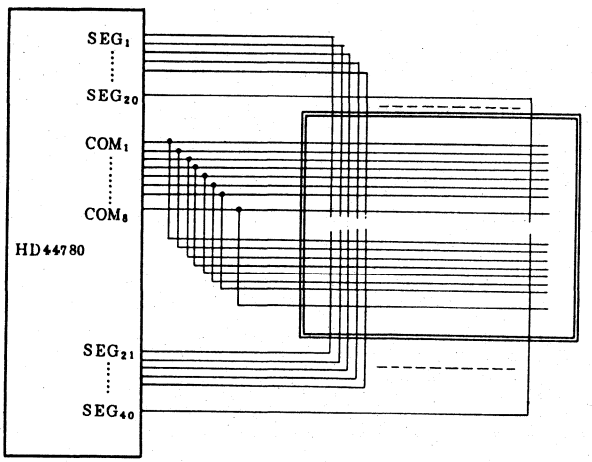
Fig. 10 Using COMg to Avoid Cross-talk on Unneeded Scanning Line

(3) Connection of Changed Matrix Layout

In the preceding examples, the number of lines was matched to the number of scanning lines. The following display types are possible by changing the matrix layout in the liquid crystal display panel.



(a) 5 ×7 dot, 16 character × 1 line Display
(1/5 Bias, 1/16 Duty)



(b) 5 ×7 dot, 4 character × 2 line Display
(1/4 Bias, 1/8 Duty)

Fig. 11 Changed Matrix Layout Displays

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters are dependent on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 characters × 1 line are the same as shown in Fig. 9.

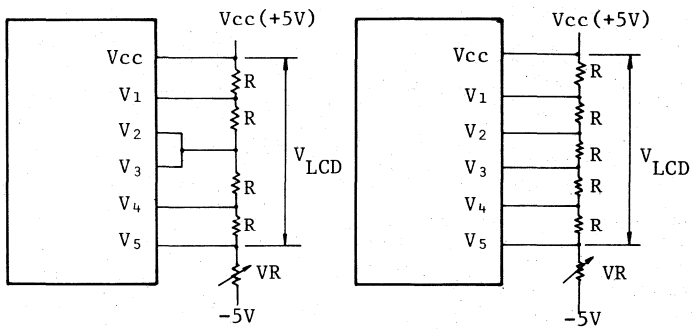
● Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44780 terminals V_1 to V_5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 6 shows the relation.

Table 6 Duty Factor and Power Supply for Liquid Crystal Display Drive

Power Supply \ Duty Factor	1/8, 1/11	1/16
Bias	1/4	1/5
V_1	$V_{cc} - \frac{1}{4}V_{LCD}$	$V_{cc} - \frac{1}{5}V_{LCD}$
V_2	$V_{cc} - \frac{1}{2}V_{LCD}$	$V_{cc} - \frac{2}{5}V_{LCD}$
V_3	$V_{cc} - \frac{1}{2}V_{LCD}$	$V_{cc} - \frac{3}{5}V_{LCD}$
V_4	$V_{cc} - \frac{3}{4}V_{LCD}$	$V_{cc} - \frac{4}{5}V_{LCD}$
V_5	$V_{cc} - V_{LCD}$	$V_{cc} - V_{LCD}$

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Fig. 13.



(a) 1/4 Bias (1/8, 1/11 Duty)

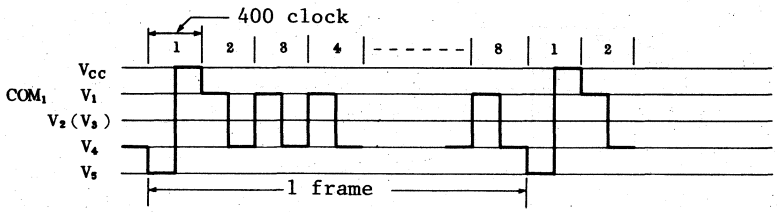
(b) 1/5 Bias (k/16 Duty)

Fig. 13 Drive Voltage Supply Example

● Relation between Oscillation Frequency and Liquid Crystal Display Frame Frequency

The following examples of liquid crystal display frame frequency apply only when oscillation frequency is 250kHz. (1 clock = 4μs)

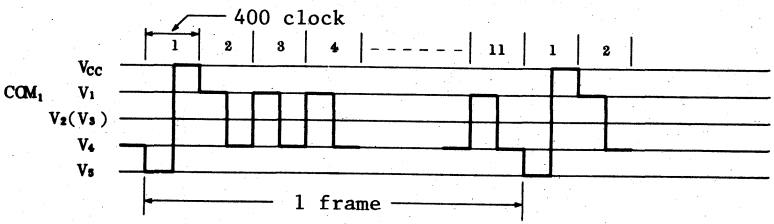
(1) 1/8 Duty



1 frame = 4 (μs) × 400 × 8 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

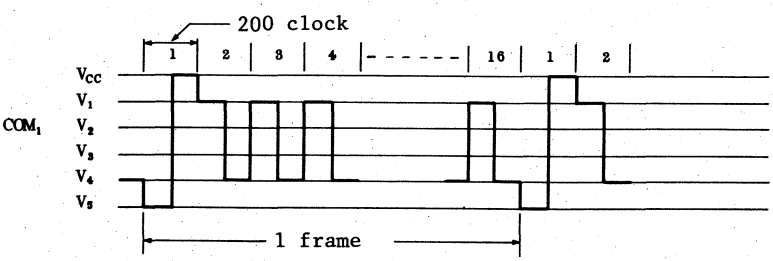
(2) 1/11 Duty



1 frame = 4 (μs) × 400 × 11 = 17600 (μs) = 17.6 (ms)

$$\text{Frame frequency} = \frac{1}{17.6\ (\text{ms})} = 56.8\ (\text{Hz})$$

(3) 1/16 Duty



1 frame = 4 (μs) × 200 × 16 = 12800 (μs) = 12.8 (ms)

$$\text{Frame frequency} = \frac{1}{12.8\ (\text{ms})} = 78.1\ (\text{Hz})$$

● Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting a liquid crystal display driver LSI HD44100H to the HD44780.

When connected to the HD44780, the HD44100H is used as segment signal driver. The HD44100H can be connected to the HD44780 directly since it supplies CL_1, CL_2, M and D signals and power for liquid crystal display drive. Fig. 14 shows a connection example.

Caution: Connection of voltage supply terminals V_1 through V_6 for liquid crystal display drive is complicated.

Up to 9 units of the HD44100H can be connected for 1-line display (duty factor 1/8 or 1/11) and up to 4 units for the 2-line display (duty factor 1/16). RAM size limits the HD44780 to a maximum of 80 character display digits. The connection method in Fig. 14 remains unchanged for both 1-line and 2-line display or both 5 ×7 and 5 ×10 dot character fonts.

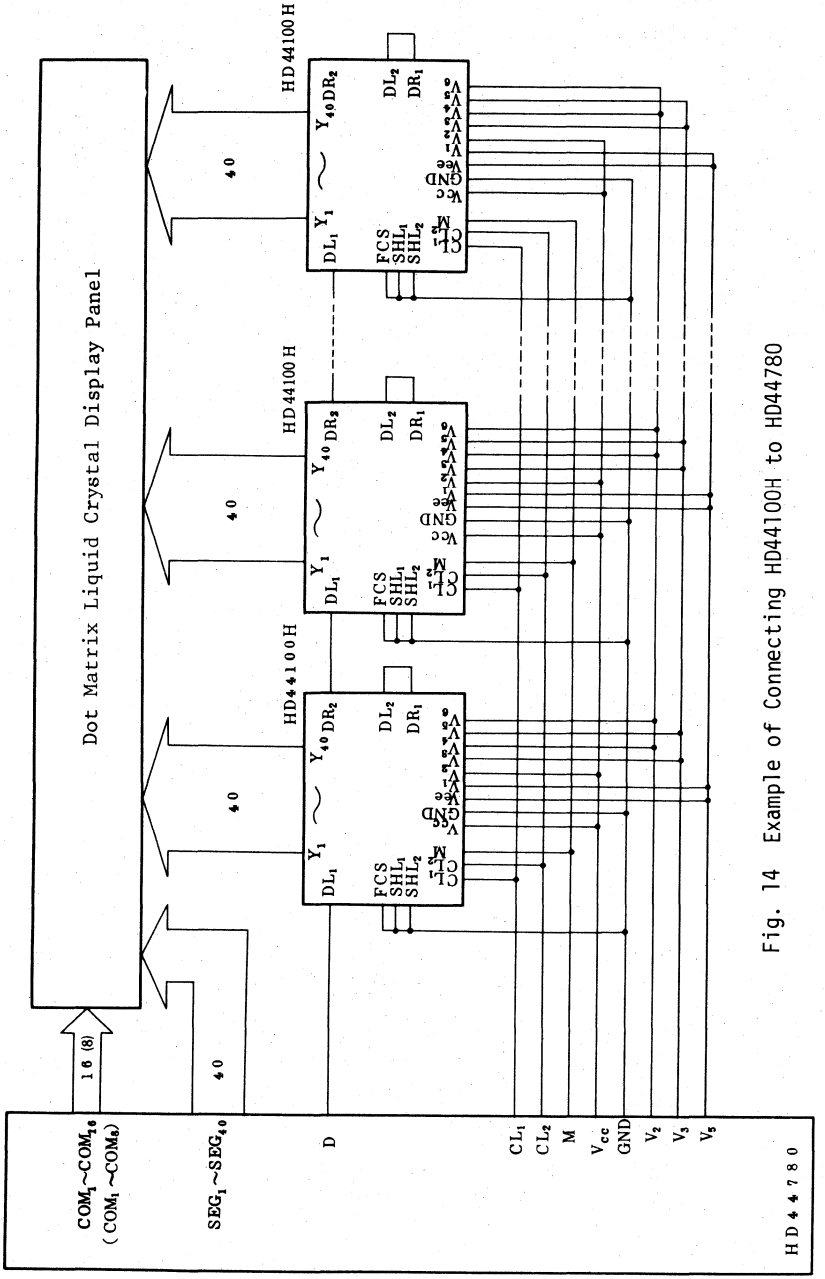


Fig. 14 Example of Connecting HD44100H to HD44780

● Instruction and Display Correspondence

(1) 8-bit operation, 8-digit × 1-line display (using internal reset)

Table 7 shows an example of 8-bit × 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

(2) 4-bit operation, 8-digit × 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. Table 8 shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is needed as a function (see Table 8).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

(3) 8-bit operation, 8-digit × 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See Table 9) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

(Note) When using the internal reset, the conditions in "Power Supply Condition Using Internal Reset Circuit" must be satisfied. If not, the HD44780 must be initialized by instruction. (See "Initializing by Instruction")

Table 7 8-bit Operation, 8-digit 1-line Display Example(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI _	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	

13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Display Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

Table 8 4-bit Operation, 8-digit 1-line Display Example
(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5×7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

Table 9 8 bit Operation, 8-digit × 2 line Display Example
(Using Internal Reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is intialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB7 DB0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5×7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0		Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0		Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Writes "H". The DD RAM has has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data co CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "O".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.

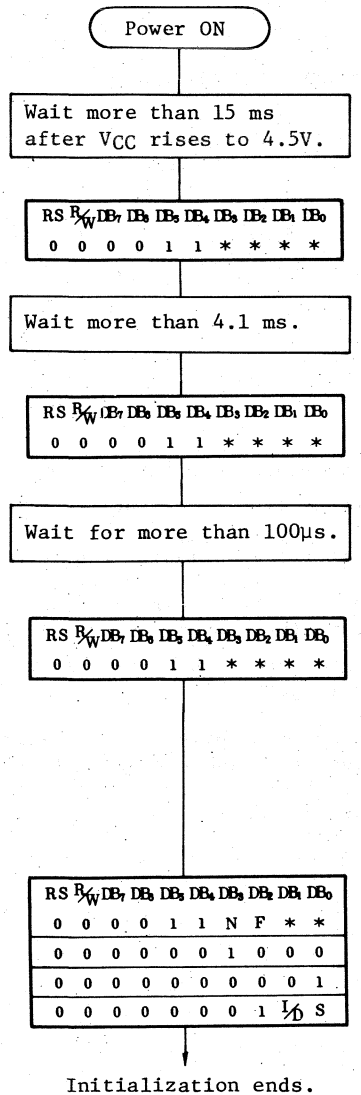
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

● Initializing by Instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long;



BF cannot be checked before this instruction.
Function set (Interface is 8 bits long.)

BF cannot be checked before this instruction.
Function set (Interface is 8 bits long.)

BF cannot be checked before this instruction.
Function set (Interface is 8 bits long.)

BF can be checked after the following instructions. When BF is not checked, the waiting time between instructions is longer than the execution instruction time. (See Table 4-1)

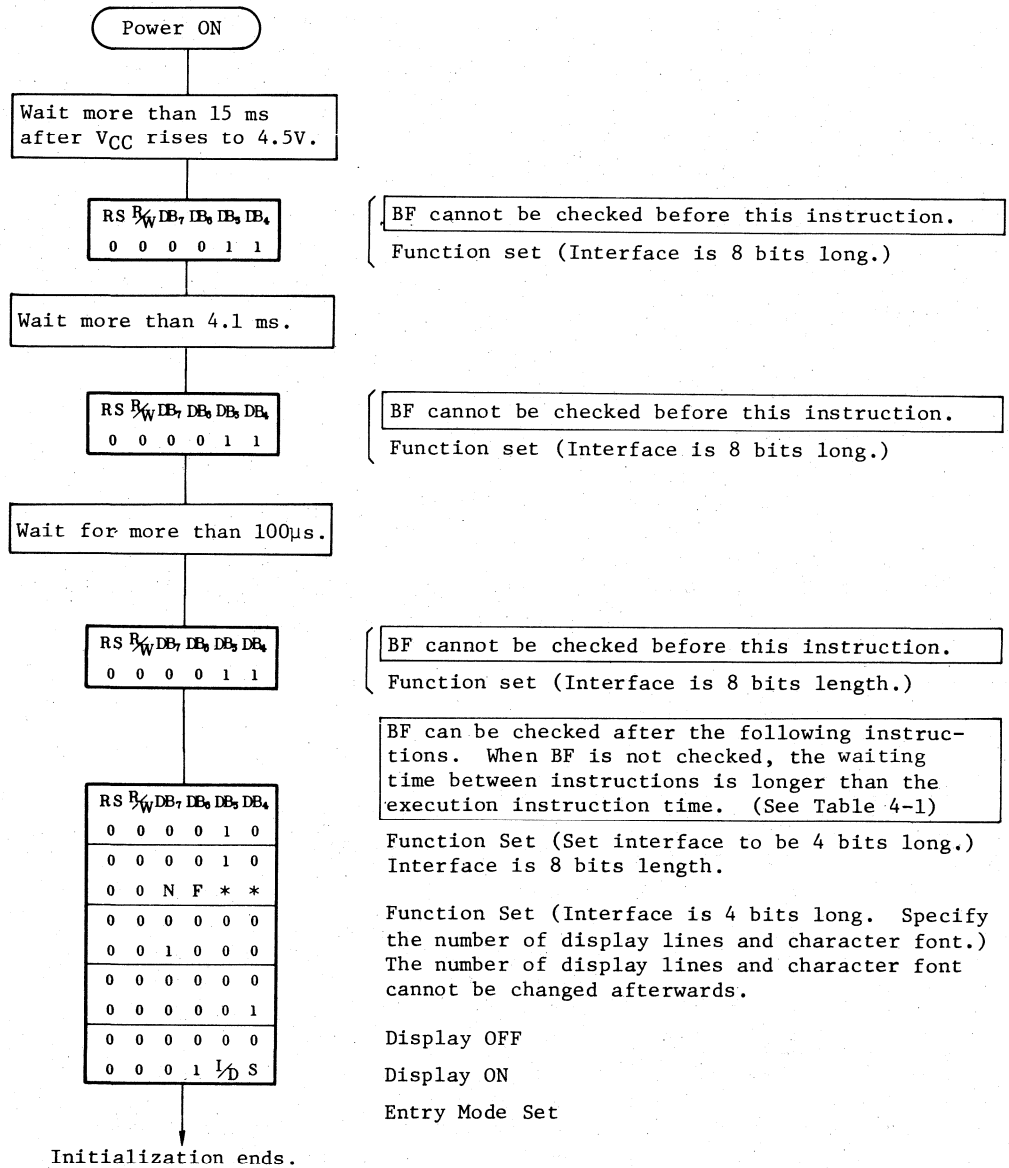
Function Set (Interface is 8 bits long. Specifiy the number of display lines and character font.)
The number of display lines and character font cannot be changed afterwards.

Display OFF

Display ON

Entry Mode Set

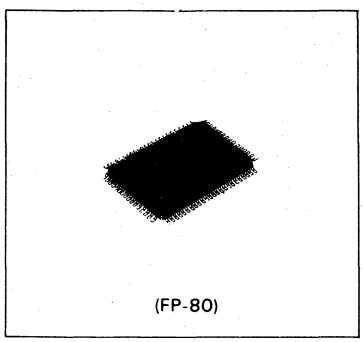
(2) When interface is 4 bits long;



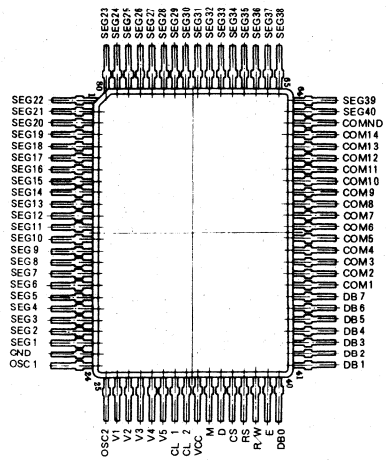
HD44101H (DOT MATRIX LIQUID CRYSTAL DISPLAY CONTROLLER & DRIVER)

The HD44101H is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are incorporated in one chip. The user can realize the dot matrix liquid crystal display system of less chip configuration by using the HD44101H.

The HD44101H is produced in the CMOS process. Therefore, the combination of HD44101H with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device making the most of its lower power dissipation.



PIN ARRANGEMENT



(Top View)

■FEATURES

- 5×7 dot matrix liquid crystal display controller & driver
- Interfaceable to 4-bit or 8-bit MPU.
- Display data RAM ... 32×8 bits (32 characters, max.)
- Character generator ROM ... 6720 bits; 192 types of 5×7 dot character font

- Internal liquid crystal display driver circuit

  15 common signal drivers

  40 segment signal drivers (can be externally extended to 120 segments by the liquid crystal display driver HD44100H)

- Duty factor (can be selected by a program)

  1/7 duty : 1 line of 5×7 dots

  1/14 duty: 2 lines of 5×7 dots

- Maximum number of display columns

No. of display lines	Duty factor	Extension	HD44101H	HD4100H	No. of display characters
1-line display	1/7 duty	Not provided	1 pc.	-----	8 characters × 1 line
		Provided	1 pc.	3 pcs. (8 characters/pc.)	32 characters × 1 line
2-line display	1/14 duty	Not provided	1 pc.	-----	8 characters × 2 lines
		Provided	1 pc.	1 pc. (8 characters × 2 lines/pc.)	16 characters × 2 lines

- Various instruction functions

  Clear Display, Return Home, Display ON/OFF, Display Shift

- Internal reset circuit at power ON

- Internal oscillator (with an external resistor)

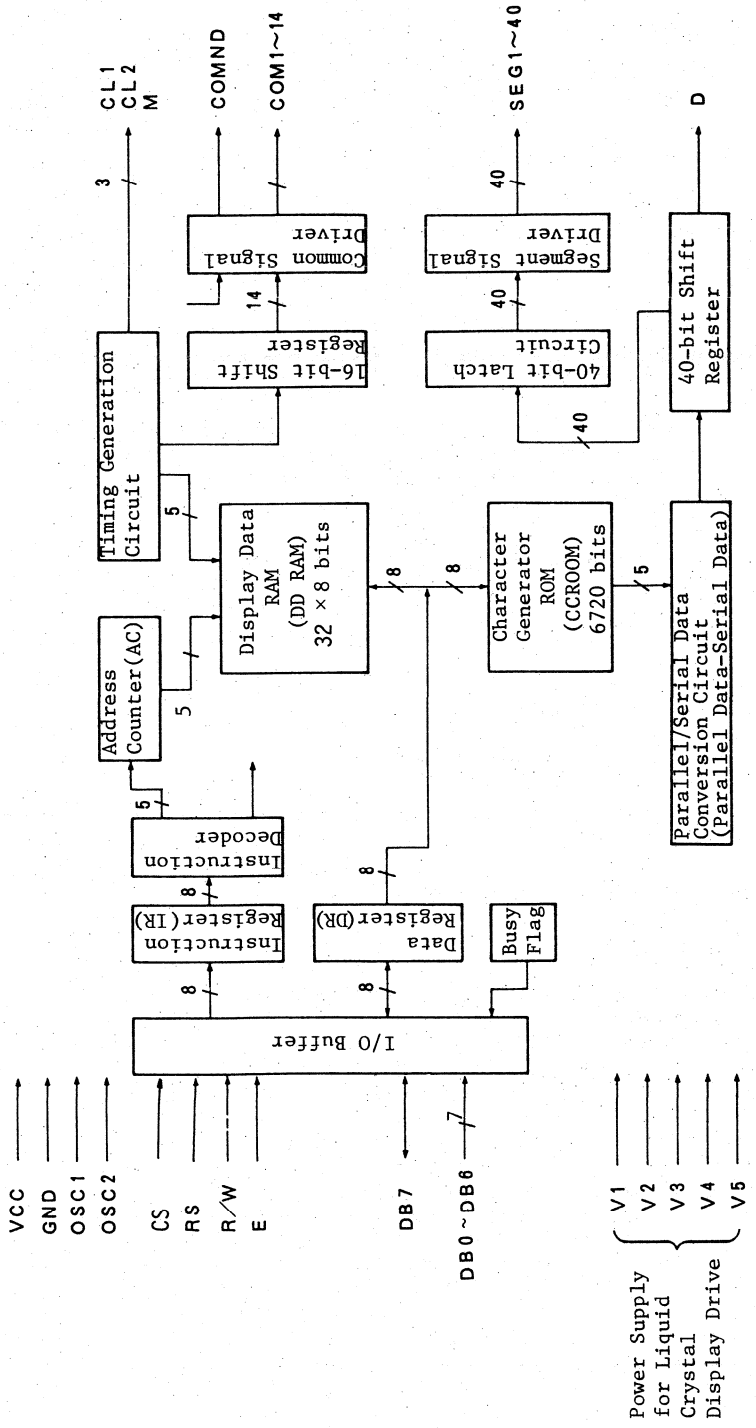
- Low power dissipation

- Logic power supply: A single +5V (excluding power for liquid crystal display drive)

- CMOS process

- 80-pin flat plastic package (FP-80)

■BLOCK DIAGRAM (HD44101H INTERIOR)



■ELECTRICAL CHARACTERISTICS

●Absolute Maximum Ratings

Item	Symbol	Limit	Unit	Note
Power supply voltage (1)	V_{CC}	-0.3 to +7.0	V	
Power supply voltage (2)	V1 to V5	V_{CC}-13.5 to V_{CC}+0.3	V	3
Input voltage	V_F	-0.3 to V_{CC}+0.3	V	
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-55 to +125	°C	

Note 1: If LSI's are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND=0V.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$.

(high ← → low)

●Electrical Characteristics

(V_{CC}=5V±10%, V5=0∿-5V, Ta=-20 to +75°C)

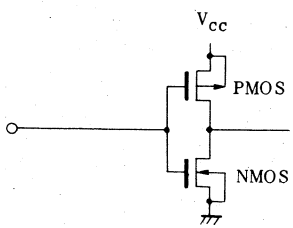
Item	Symbol	Test condition	Limit			Unit	Note
			Min.	Type	Max.		
Input "high" voltage (1)	$V_{IH(1)}$		2.0	-	V_{CC}	V	(2)
Input "low" voltage (1)	$V_{II(1)}$		0	-	0.8	V	(2)
Output "high" voltage (TTL)	V_{OH}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "low" voltage (TTL)	V_{OL}	I_{OL}=1.6mA	-	-	0.4	V	(3)
Output "high" voltage (CMOS)	VOHC	$-I_{OH}$=0.1mA	V_{CC}-0.4	-	-	V	(4)
Output "low" voltage (CMOS)	V_{OLC}	I_{OL}=0.1mA	-	-	0.4	V	(4)
Driver voltage descending(COM)	V_{d1}	Id=0.1mA	-	-	1.0	V	
Driver voltage descending(SEG)	V_{d2}	Id=0.01mA	-	-	0.2	V	
Input leakage current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	μA	(5)
Pull up MOS current	$-I_P$	V_{CC}=5V, V_{IN}=0V Ta=25°C	2	10	20	μA	

Item	Symbol	Test condition	Limit			Unit	Note
			Min.	Type	Max.		
Power supply current	I_{CC}	R_f oscillation, External clock operation fosc=fcp=78kHz	-	0.2	0.5	mA	(6)
External clock operation							
External clock frequency	f_{cp}		40	78	150	kHz	(7)
External clock duty	Duty		45	50	55	%	(7)
External clock rise time	t_{rcp}		-	-	0.2	µs	(7)
External clock fall time	t_{fcp}		-	-	0.2	µs	(7)
Input "high" voltage (2)	V_{IH2}		V_{CC}-1.0	-	V_{CC}	V	(8)
Input "low" voltage (2)	V_{IL2}		0	-	1.0	V	(8)
Internal clock operation (Rf oscillation)							
Clock oscillation frequency	f_{osc}	Rf=560kΩ±2%	50	75	100	kHz	(9)

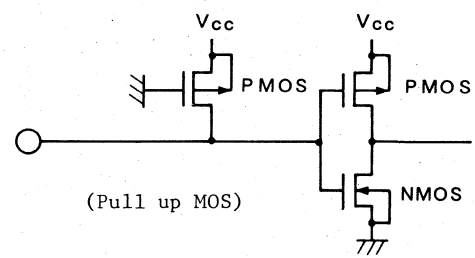
Note 1: The following are I/O terminal configurations except for liquid crystal display output.

Input Terminal

Applicable terminals: E
(No pull up MOS)

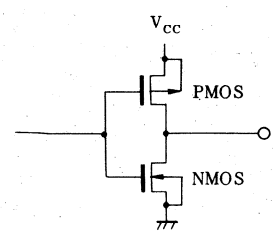


Applicable terminals: RS, R/W, CS, DB0 to DB6
(With pull up MOS)



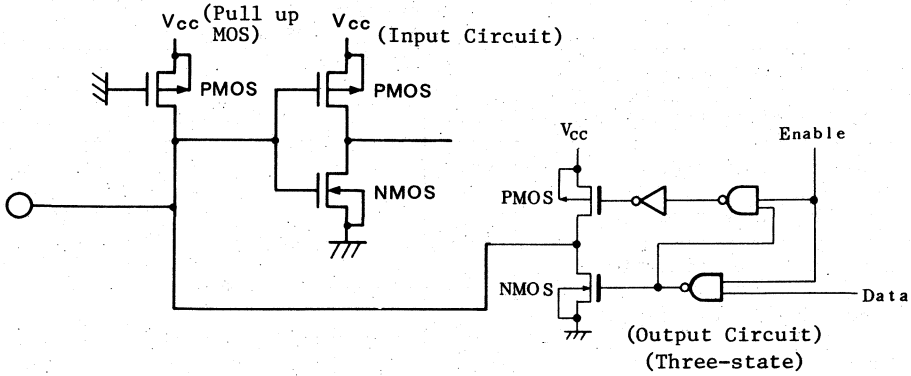
· Output Terminal

Applicable terminals: CL1, CL2, M, D



• I/O Terminals

Applicable terminals: DB7



Note 2: Input terminals and I/O terminals
Excludes OSC1 terminals.

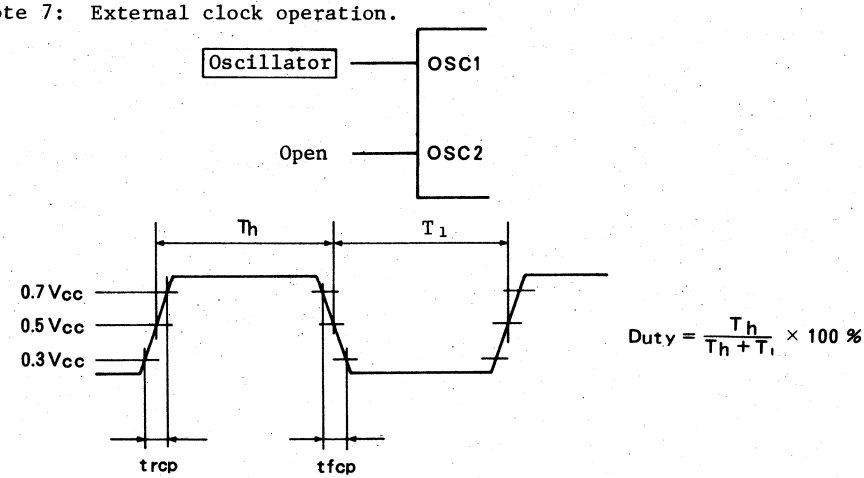
Note 3: I/O terminals

Note 4: Output terminals

Note 5: Current flowing through pull-up MOS's and output drive MOS's is excluded.

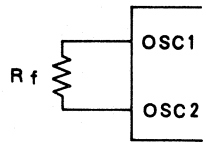
Note 6: Input/output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

Note 7: External clock operation.



Note 8: Applied to OSC1 terminal.

Note 9: Internal oscillator operation using oscillation resistor Rf.



Rf: 560kΩ±2%

Since oscillation frequency varies depending on OSC_1 and OSC_2 terminal capacity, wiring length for these terminals should be minimized.

●Timing Characteristics

Write Operation

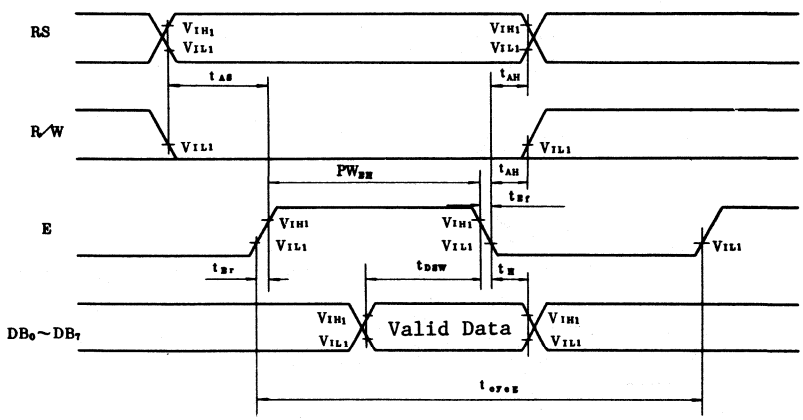


Fig. 1 Bus Write Operation Sequence
(Writing Data from MPU to HD44101H)

Read Operation

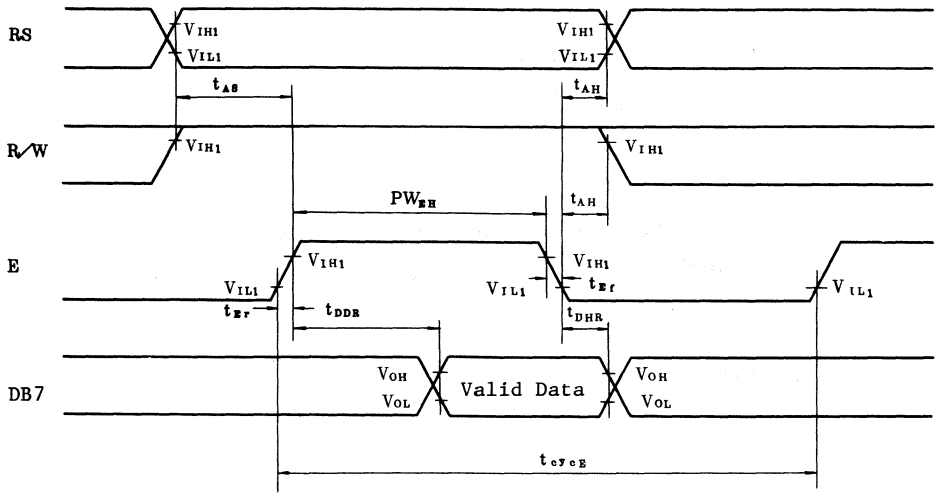


Fig. 2 Bus Read Operation Sequence
(Reading out Data from HD44101H to MPU)

Interface Signal with Driver LSI HD44100H

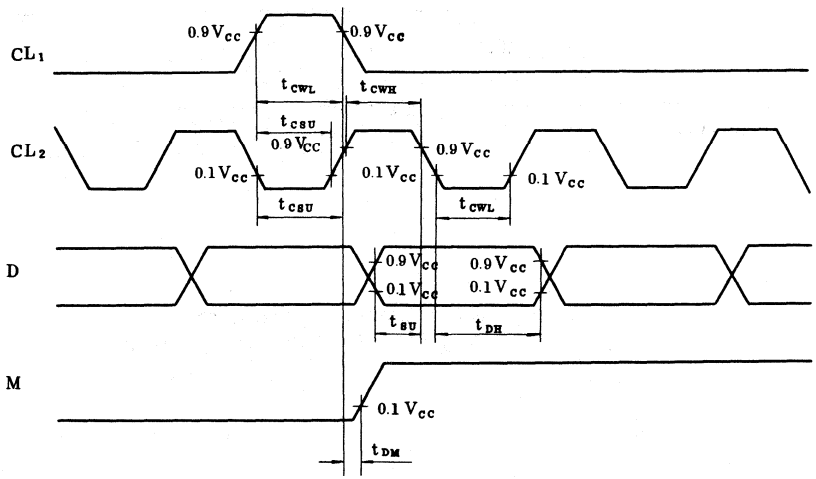


Fig. 3 Sending Data to Driver LSI HD44100H

● Bus Timing Characteristics

(V_{CC}=5.0V±10%, GND=0V, Ta=-20 to +75°C)

Write Operation (Writing data from MPU to HD44101H)

Item		Symbol	Test conditions	Limit		Unit
				Min.	Max.	
Enable cycle time		$T_{cyc}E$	Fig. 1	1000	-	ns
Enable pulse width	"High" level	PW_{EH}	Fig. 1	450	-	ns
Enable rise/fall time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address set-up time	RS, R/W — E	t_{AS}	Fig. 1	140	-	ns
Address hold time		t_{AH}	Fig. 1	10	-	ns
Data set-up time		t_{DSW}	Fig. 1	195	-	ns
Data hold time		t_H	Fig. 1	10	-	ns

Read Operation (Reading data from HD44101H to MPU)

Item		Symbol	Test conditions	Limit		Unit
				Min.	Max.	
Enable cycle time		$t_{cyc}E$	Fig. 2	1000	-	ns
Enable pulse width	"High" level	PW_{EH}	Fig. 2	450	-	ns
Enable rise/fall time		t_{Er}, t_{Ef}	Fig. 2	-	25	ns
Address set-up time	RS, R/W — E	t_{AS}	Fig. 2	140	-	ns
Address hold time		t_{AH}	Fig. 2	10	-	ns
Data delay time		t_{DDR}	Fig. 2	-	320	ns
Data hold time		t_{DHR}	Fig. 2	20	-	ns

● Interface Signal with HD44100H Timing Characteristics

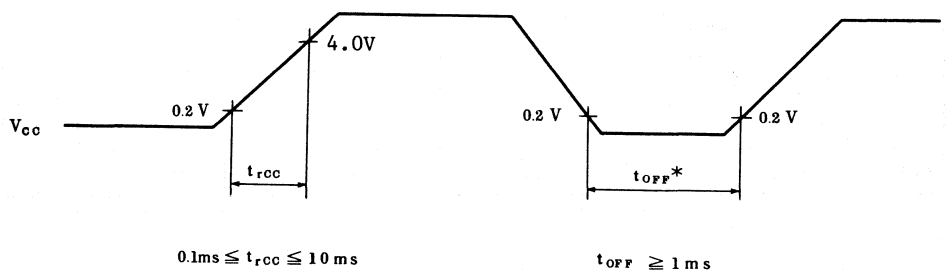
(V_{CC}=5.0V±10%, GND=0V, Ta=-20 to +75°C)

Item		Symbol	Test conditions	Limit		Unit
				Min.	Max.	
Clock pulse width	"High" level	t_{CWH}	Fig. 3	800	-	ns
Clock pulse width	"High" level	t_{CWL}	Fig. 3	800	-	ns
Clock set-up time		t_{CSU}	Fig. 3	500	-	ns
Data set-up time		t_{SU}	Fig. 3	300	-	ns
Data hold time		t_{DH}	Fig. 3	300	-	ns
M delay time		t_{DM}	Fig. 3	-1000	1000	ns

● Power Supply Conditions Using Internal Reset Circuit

Item	Symbol	Test conditions	Limit		Unit
			Min.	Max.	
Power supply rise time	t_{rcc}	-	0.1	10	ms
Power supply OFF time	t_{OFF}	-	1	-	ms

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction.



0.1ms ≦ t_{rcc} ≦ 10 ms $\qquad$ t_{OFF} ≧ 1 ms

(Note) t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.

■TERMINAL FUNCTION

Table 1 Functional Description of Terminals

Signal name	Number of lines	Input/ output	Connected to	Function
RS	1	Input	MPU	Signal to select registers "0": Instruction register (for write) Busy flag (for read) "1": Data register (for read and write)
R/W	1	Input	MPU	Signal to select read (R) and write (W) "0": Write "1": Read
E	1	Input	MPU	Operation start signal for data read/write
DB4 ∿DB7	4	Input, I/O only DB7	MPU	Higher order 4 lines data bus. Used for data transfer between the MPU and the HD44101H. DB7 can be used as a BUSY flag.
DB0 ∿DB3	4	Input	MPU	Lower order 4 lines data bus. Used for data transfer from the MPU to the HD44101H. These four are not used during 4-bit operation.
CL_1	1	Output	HD44100H	Clock to latch serial data D sent to the driver LSI HD44100H.
CL_2	1	Output	HD44100H	Clock to shift serial data D.
M	1	Output	HD44100H	Switch signal to convert liquid crystal drive waveform to AC.
D	1	Output	HD44100H	Character pattern data corresponding to each common signal is serially sent. "0": Non selection "1": Selection
COM1 ∿COM14	14	Output	Liquid crystal display	Common signals that are not used are changed to non-selection waveforms. That is, COM8∿COM14 are in non-selection waveform at 1/7 duty factor.
SEG1 ∿SEG40	40	Output	Liquid crystal display	Segment signal
V1∿V5	5		Power supply	Power supply for liquid crystal display drive
V_{CC}, GND	2		Power supply	V_{CC}: +5V, GND: 0V
OSC_1, OSC_2	2			Terminals connected to resistor for internal clock oscillation. For external clock operation, the clock is input to OSC_1.
COMND	1	Output	Liquid crystal display	Non-selected common signal. It is applied to unused common terminals of LCD, if necessary.

Signal name	Number of lines	Input/ output	Connected to	Function
CS	1	Input	MPU	Chip select signal "0": Disable "1": Enable

■FUNCTION OF EACH BLOCK

(1) Register

The HD44101H has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and display ON/OFF, and address information for display data RAM (DD RAM). The IR can be written from the MPU, but can not be read.

The DR temporarily stores data to be written into the DD RAM. Data written into the DR from the MPU is automatically written into the DD RAM by internal operation. The DR can be also written from the MPU, but can not be read. Register selector (RS) signals make their selection from these two registers.

Table 2 Register Selection

RS	R/W	Operation
0	0	IR write as internal operation (Display clear, etc.)
0	1	Read busy flag (DB7)
1	0	DR write as internal operation (DR to DD RAM)

(2) Busy flag (BF)

When the busy flag is "1", the HD44101H is in the internal operation mode, and the next instruction will not be accepted. As Table 2 shows, the busy flag is output to DB7, when RS=0 and R/W=1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

The address counter (AC) assigns addresses to DD RAM. When an instruction for address is written in IR, the address information is sent from IR to AC.

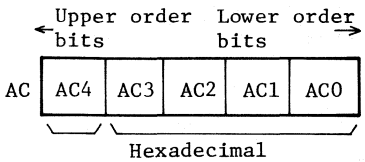
After writing into DD RAM display data, AC is automatically increased by +1.

(4) Display data RAM (DD RAM)

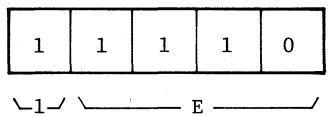
The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 32×8 bits, or 32 characters.

Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

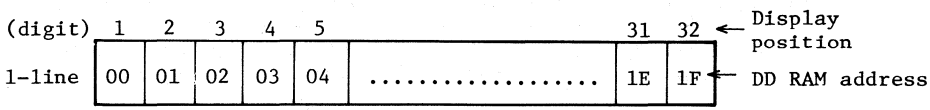
The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



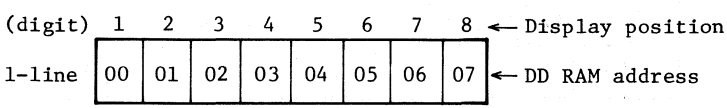
(Example) DD RAM address "1E"



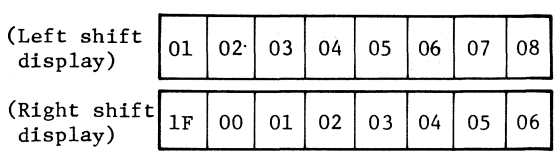
1-line display (N=0)



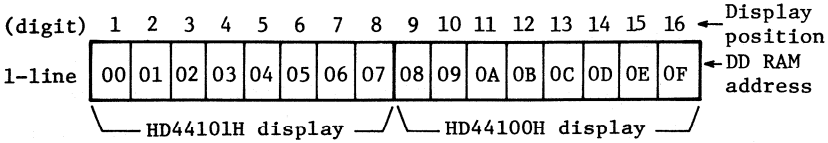
(a) When the display characters are less than 32, the display begins at the head position. For example, 8 characters using 1 HD44101H are displayed as:



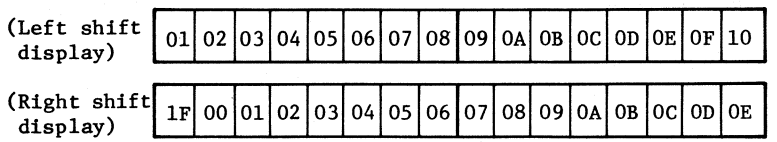
When the display shift operation is performed, the DD RAM address moves as:



(b) 16-character display using an HD44101H and an HD44100H is as shown below:

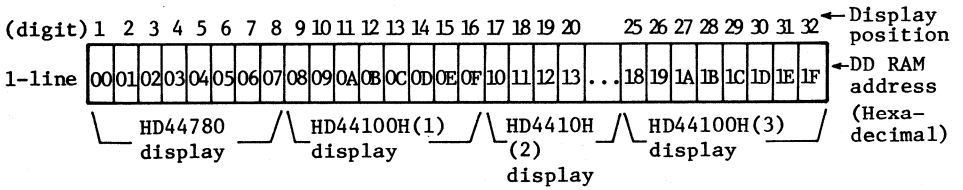


When the display shift operation is performed, the DD RAM address moves as:

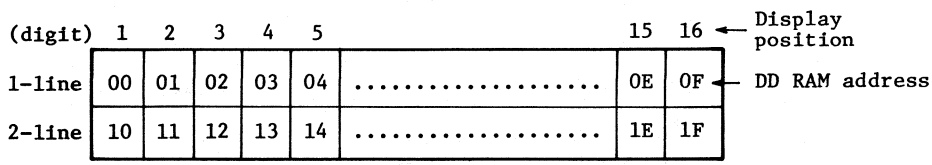


(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44101H and two or more HD44100H's can be considered an extension of (b).

Since the increase can be 8 digits for each additional HD44100H, up to 32 digits can be displayed by externally connecting 3 HD44100H's.



• 2-line display (N=1)



(a) When the number of display characters is less than 16×2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44101H is used, 8 characters×2 lines are displayed as:

(digit)	1	2	3	4	5	6	7	8	← Display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address
2-line	10	11	12	13	14	15	16	17	

When display shift is performed, the DD RAM address moves as:

(Left shift display)	01	02	03	04	05	06	07	08
	11	12	13	14	15	16	17	18

(Right shift display)	0F	00	01	02	03	04	05	06
	1F	10	11	12	13	14	15	16

(b) 16 characters × 2 lines are displayed when an HD44101H and an HD44100H are used:

(digit)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address
2-line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	

HD44101H display — HD4410H display

When display shift is performed, the DD RAM address moves as follows:

(Left shift display)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00
	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10

(Right shift display)	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

(5) Character generator ROM (CG ROM)

The character generator ROM generates 5×7 dot character patterns from 8-bit character codes. It can generate 192 types of 5×7 dot character patterns. Table 3 shows the relation between character codes and character patterns in the Hitachi standard HD44101A00H. User defined character patterns are also available by mask-programming ROM.

Table 3 Correspondence between Character Codes and Character Patterns (Hitachi Standard HD44101A00H)

Higher / Lower 4bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000												
××××0001												
××××0010												
××××0011												
××××0100												
××××0101												
××××0110												
××××0111												
××××1000												
××××1001												
××××1010												
××××1011												
××××1100												
××××1101												
××××1110												
××××1111												

(6) Timing generation circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(7) Liquid crystal display driver circuit

The liquid crystal display driver circuit consists of 14 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms.

The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension.

Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44101H drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

COMND always outputs non-selected common waveform. This signal can be applied to unused common lines in the LCD panel, if necessary, and all the picture element on this common are not visible (see Fig. 10).

■RESET FUNCTION

The HD44101H automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. The busy stats is 15 ms after V_{CC} rises to 4.0V.

(1) Display clear

(2) Function set ..... DL=0: 4 bit long interface data
N=0 : 1-line display

(3) Display ON/OFF control ..... D=0 : Display OFF

(Note) When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit will not operate normally and initialization will not be performed.

■INSTRUCTION

●Outline

Only two HD44101H registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44101H internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44101H internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals (DB0 ∿ DB7), and are called instructions, here.

Table 4 shows the instructions. Details are explained in subsequent sections. Instructions are of 4 types, those that,

(1) Designate HD44101H functions such as display format, data length, etc.
(2) Give internal RAM addresses.
(3) Perform data transfer to internal RAM.
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic increasing by +1 of HD44101H internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programming efficiency.

For an explanation of the shift function in its relation to display, see Table 6.

When an instruction is executing during internal operation, no instruction other than the busy flag read instruction will be executed. Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "0" before sending an instruction from the MPU.

Table 4 Instructions

Instruction	Code										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.
Return home	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.
Display ON/OFF control	0	0	0	0	0	0	1	D	*	*	Sets ON/OFF of entire display (D).
Display shift	0	0	0	0	0	1	1	R/L	*	*	Shifts display without changing DD RAM contents.
Function set	0	0	0	0	1	DL	N	*	*	*	Sets interface data length (DL), number of display lines (L).
Set DD RAM address	0	0	1	0	0	$(A_{DD})_B$					Sets DD RAM address. DD RAM data is received after this setting.
Read busy flag	0	1	BF	*	*	*	*	*	*	*	Reads busy flag (BF) indicating internal operation is being performed.
Write data to DD RAM	1	0	$(\text{Write data})_B$								Writes data into DD RAM.
	D=1: Display on D=0: Display off R/L=1: Shift to the right R/L=0: Shift to the left DL=1: 8 bits, DL=0: 4 bits N=1: 2 lines, N=0: 1 line BF=1: Internally operating BF=0: Can accept instruction										DD RAM: Display data RAM A_{DD}: DD RAM address AC : Address counter used for DD RAM address

* No effect

● Description of Details

(1) Clear display

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal)(character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears.

(2) Return home

	RS	R/W	DB7						DB0	
Code	0	0	0	0	0	0	0	0	1	*

* Don't care.

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change.

(3) Display ON/OFF control

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	1	D	*	*

D: The display is ON when D=1 and OFF when D-0. When off due to D=0, display data remains in the DD RAM. It can be displayed immediately by setting D=1.

(4) Display shift

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	1	1	R/L	*	*

* Don't care.

Shifts display to the right or left without writing display data. This function is used to correct or search for the display. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

R/L=0: Shifts the entire display to the left.
R/L=1: Shifts the entire display to the right.

Address counter (AC) contents do not change if the only action performed is shift display.

(5) Function set

	RS	R/W	DB7							DB0
Code	0	0	0	0	1	DL	N	*	*	*

* Don't care.

DL: Sets interface data length. Data is sent or received in 8 bit lengths (DB7∿DB0) when DL=1 and in 4 bit lengths (DB7∿DB4) when DL=0. When the 4 bit length is selected, data must be sent or received twice.

N : Sets number of display lines.

N	No. of display lines	Character font	Duty factor
0	1	5×7 dots	1/7
1	2	5×7 dots	1/14

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

(6) Set DD RAM address

	RS	R/W	DB7							DB0
Code	0	0	1	0	0	A	A	A	A	A

Higher order bits — Lower order bits →

Set the DD RAM address into the address counter in binary AAAAA. Data is then written from the MPU for the DD RAM.

However, when N=0 (1-line display), AAAAA is "00"∿"1F" (hexadecimal)
When N=1 (2-line display), AAAAA is "00"∿"0F" (hexadecimal) for the first line, and "10"∿"1F" (hexadecimal) for the second line.

(7) Read busy flag

	RS	R/W	DB7						DB0
Code	0	1	BF	*	*	*	*	*	*	*

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF=1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next write operation.

(8) Write data to DD RAM

	RS	R/W	DB7						DB0
Code	1	0	D	D	D	D	D	D	D	D

← Higher order bits Lower order bits →

Writes binary 8 bit data DDDDDDDD to the DD RAM.
Where the DD RAM is to be written into is determined by the previous specification of DD RAM address setting. After write, the address is automatically increased by 1.

* Instruction cycle time = $\frac{5}{f_{OCS}}$ or $\frac{5}{f_{CP}}$

■HOW TO USE THE HD44101H

●Interface to MPU

(1) Interface to 8-bit MPU

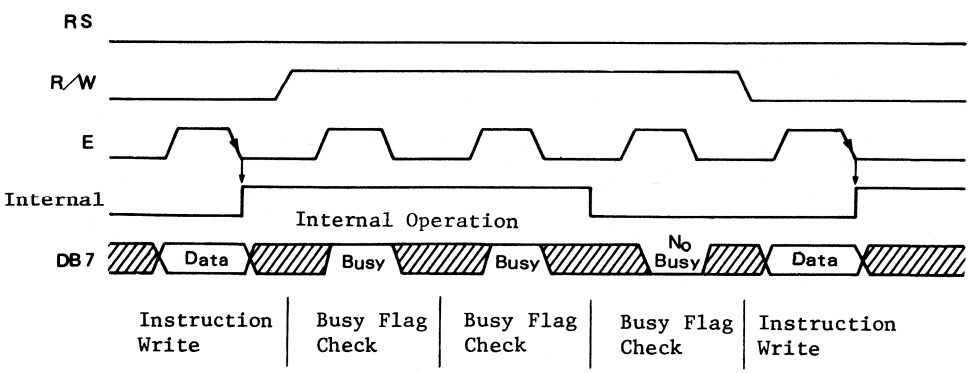


Fig. 4 Example of Busy Flag Check Timing Sequence

① Direct interface to HD6800

The HD44101H can interface directly to the 8-bit MPU HD6800, having the capability of driving one ordinary TTL through the TTL compatible interface. The interface timing is matched with the HD6800. However, the HD44101H's internal operation is slow, an access must be made while checking the busy signal. Fig. 5 shows an example of circuit. In the example, the HD44100H is selected with A14=1, A15=0 and the timing width is obtained by VMA and $\phi 2$.

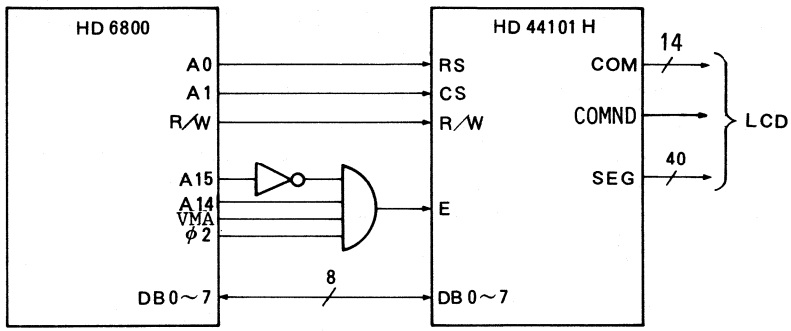
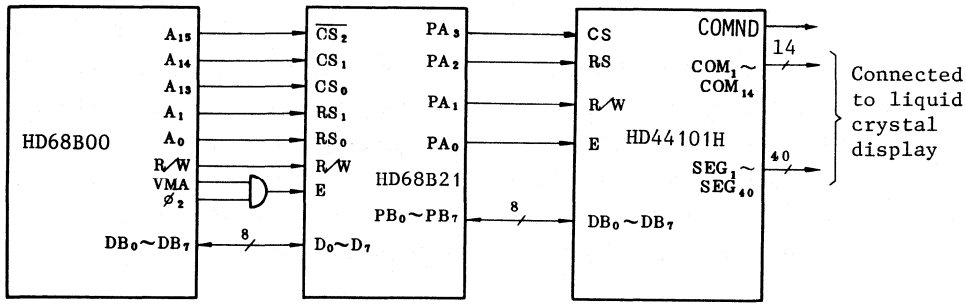


Fig. 5 Example of Interface to HD6800

② When connecting to 8-bit MPU through PIA

Fig. 6 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

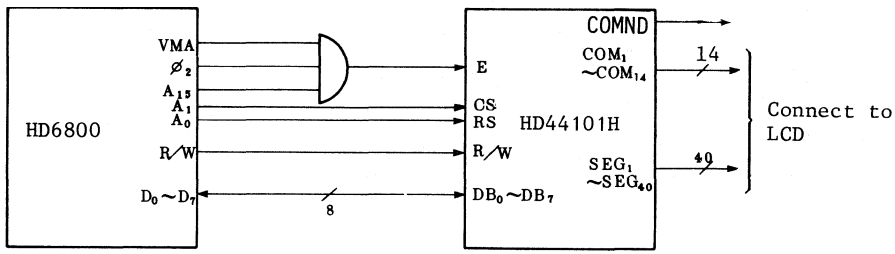
In the example, PB0 to PB7 are connected to the data buses DB0 to DB7 and PA0 to PA3 are connected to E, R/W, RS and CS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.



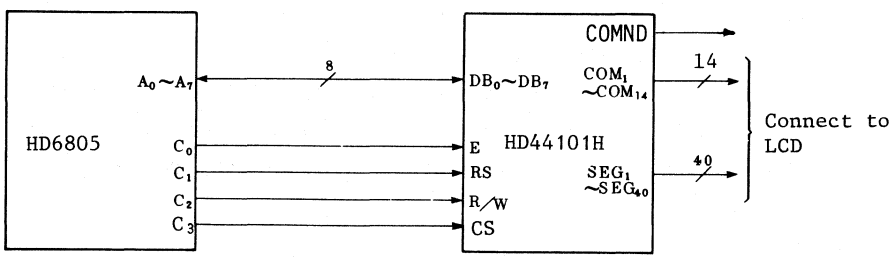
HD68B00: 8 bit CPU

Fig. 6 Example of Interface to HD68B00 Using PIA (HD68B21)

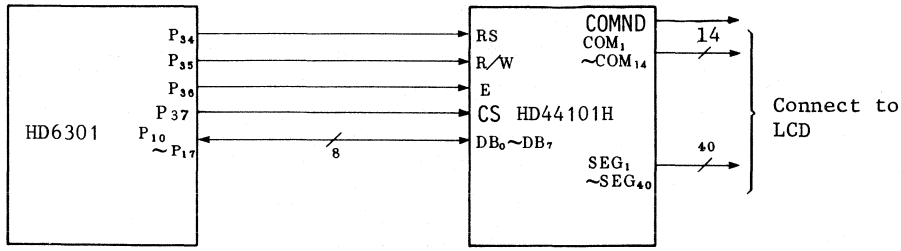
③ Connecting directly to the 8-bit MPU bus line



④ Example of interfacing to the HD6805



⑤ Example of interfacing to the HD6301

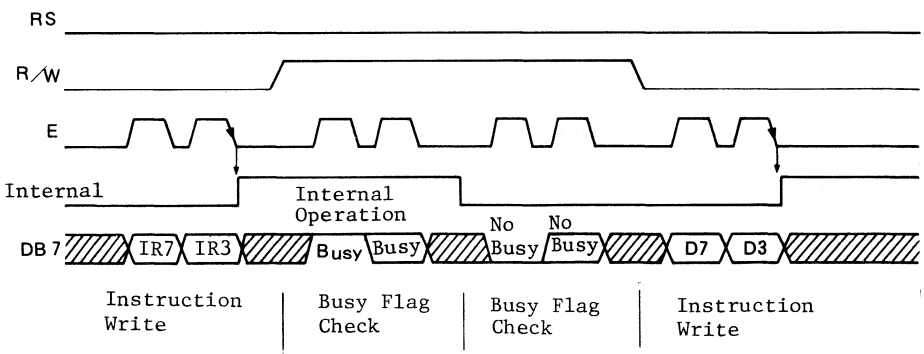


(2) Interface to 4-bit MPU

The HD44101H can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex (see Fig. 7).

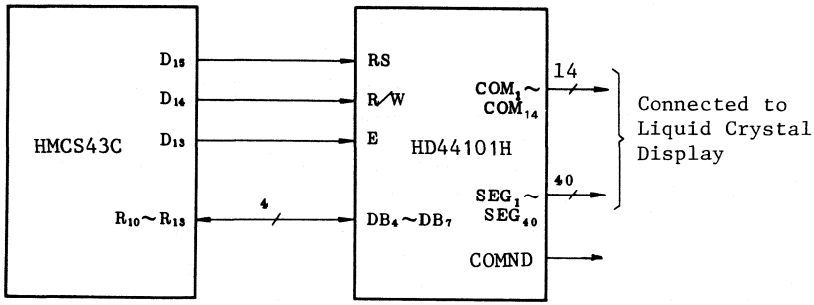
Fig. 8 shows an example of interface to the HMCS43C.

Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.



Note: IR7, IR3: Instruction 7th bit, 3rd bit

Fig. 7 An Example of 4-bit Data Transfer Timing Sequence



HMCS43C: Hitachi 4-bit single-chip microcomputer

Fig. 8 Example of Interface to the HMCS43C

●Interface to Liquid Crystal Display

(1) Character font and number of lines

The HD44101H can perform 5×7 dots as character font.

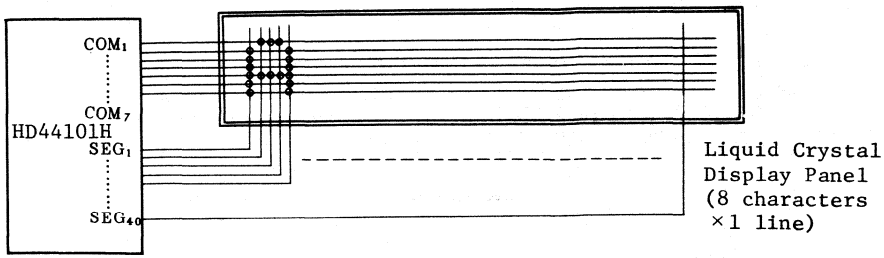
Up to 2 lines are displayed with 5×7 dots. Therefore, two types of common signals are available:

Number of lines	Character font	Number of common signals	Duty factor
1	5×7 dots	7	1/7
2	5×7 dots	14	1/14

Number of lines and font types can be selected by program.
(See Table $\overline{4}$, Instruction.)

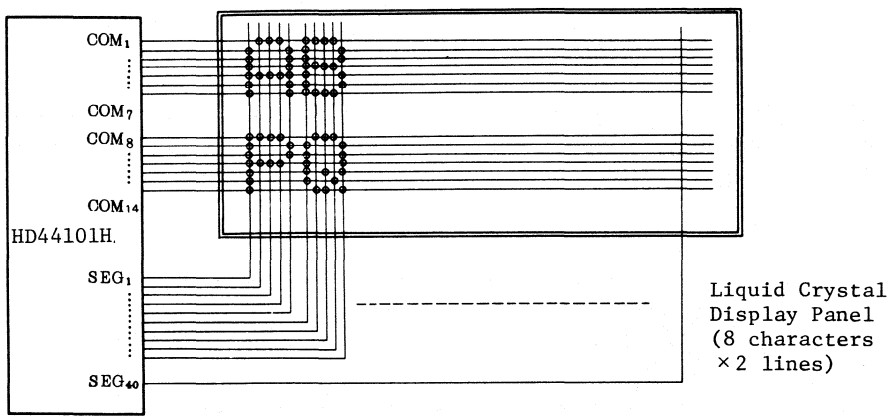
(2) Connection to HD44101H and liquid crystal display

Fig. 9 (1) and (2) show connection examples.



Example of a 5×7 dot, 8 character × 1 line display (1/4 bias, 1/7 duty)

Fig. 9 (1) Liquid Crystal Display and Connections to HD44101H

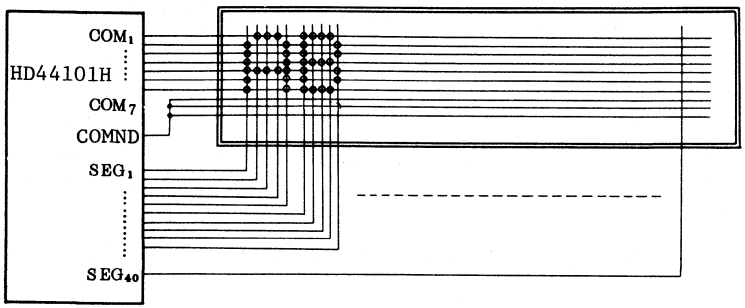


Example of 5×7 dot, 8 character × 2 line display (1/5 bias, 1/14 duty)

Fig. 9 (2) Liquid Crystal Display and Connection to HD44101H

Since 5 signal lines at the SEG can display one digit, one HD44101H can display up to 8 digits for 1-line display and 16 digits for 2-line display.

In Fig. 9 (1) (2), there are unused common signal terminals, non-selection waveforms which always output. When the liquid crystal display panel has unused extra scanning lines, avoid undesirable influences due to cross-talk in the floating state by connecting the extra scanning lines to these common signal terminals.

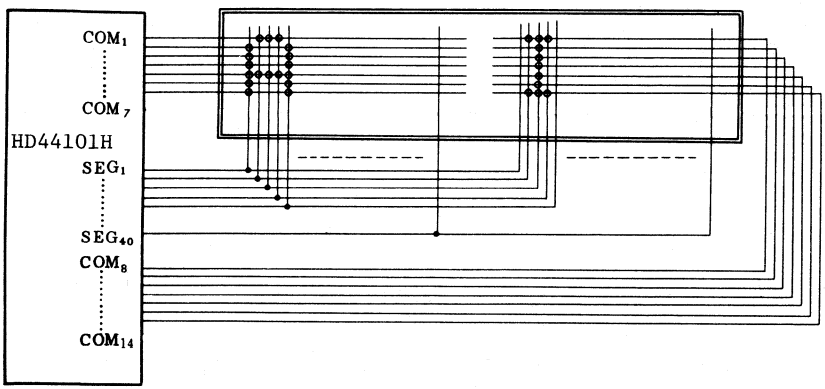


5×7 dot, 8 character × 1 line display (1/4 bias, 1/7 duty)

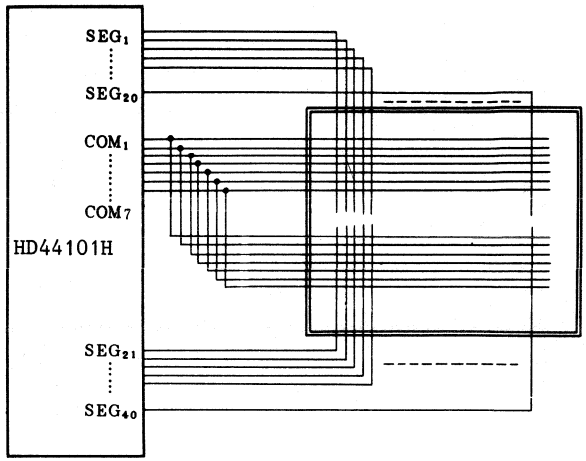
Fig. 10 Using COMND to Avoid Cross-Talk on Unneeded Scanning Line

(3) Connection of changed matrix layout

In the preceding examples, the number of lines was matched to the number of scanning lines. The following display types are possible by changing the matrix layout in the liquid crystal display panel.



(a) 5×7 dot, 16 character × 1 line display (1/5 bias, 1/14 duty)



(b) 5×7 dot, 4 character × 2 line display (1/4 bias, 1/7 duty)

Fig. 11 Changed Matrix Layout Displays

In either case, the only change is the layout. Display characteristics and the number of liquid crystal display characters are dependent on the number of common signals (or duty factor). Note that the display data RAM (DD RAM) addresses for 8 characters × 2 lines and 16 character × 1 line are the same as shown in Fig. 9.

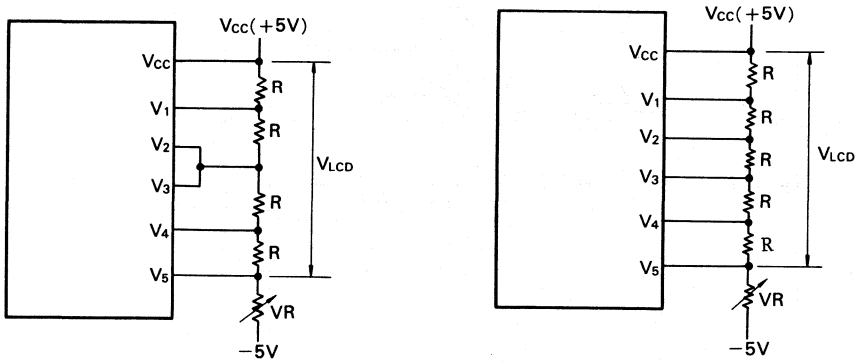
● Power Supply for Liquid Crystal Display Drive

Various voltage levels must be applied to HD44101H terminals V1 to V5 to obtain liquid crystal display drive waveforms. The voltages must be changed according to duty factor. Table 5 shows the relation.

Table 5 Duty Factor and Power Supply for Liquid Crystal Display Drive

Duty factor	1/7	1/14
Power supply \ Bias	1/4	1/5
V1	$V_{CC} - 1/4V_{LCD}$	$V_{CC} - 1/5V_{LCD}$
V2	$V_{CC} - 1/2V_{LCD}$	$V_{CC} - 2/5V_{LCD}$
V3	$V_{CC} - 1/2V_{LCD}$	$V_{CC} - 3/5V_{LCD}$
V4	$V_{CC} - 3/4V_{LCD}$	$V_{CC} - 4/5V_{LCD}$
V5	$V_{CC} - V_{LCD}$	$V_{CC} - V_{LCD}$

V_{LCD} gives the peak values for liquid crystal display drive waveforms. Resistance dividing provides each voltage as shown in Fig. 12.



(a) 1/4 bias (1/7 duty) (b) 1/5 bias (1/14 duty)

Fig. 12 Drive Voltage Supply Example

● Connection with Driver LSI HD44100H

You can increase the number of display digits by externally connecting a liquid crystal display driver LSI HD44100H to the HD44101H.

When connected to the HD44101H, the HD44100H is used as segment signal driver. The HD44101H can be connected to the HD44100H directly since it supplies CL1, CL2, M and D signals and power for liquid crystal display drive. Fig. 13 shows a connection example.

Caution: Connection of voltage supply terminals V1 through V6 for liquid crystal display drive is complicated.

Up to 3 units of the HD44100H can be connected for 1-line display (duty factor 1/7) and up to 1 unit for the 2-line display (duty factor 1/14). RAM size limits the HD44101H to a maximum of 32 character display digits. The connection method in Fig. 13 remains unchanged for both 1-line and 2-line display.

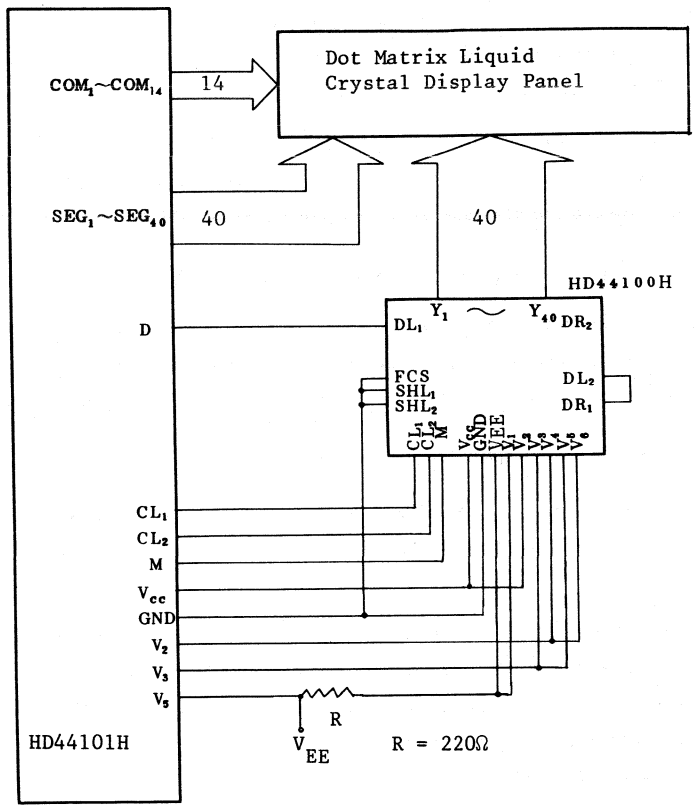


Fig. 13 Example of Connecting HD44100H to HD44101H

●Instruction and Display Correspondence

(1) 8-bit operation, 8-digit × 1-line display

Table 6 shows an example of 8-digit X 1-line display in 8-bit operation. The HD44101H functions must be set by Function Set prior to display. Since the display data RAM can store data for 32 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

(2) 4-bit operation, 8-digit × 1-line display

Table 7 shows an example of 8-digit X 1-line display in 4-bit operation. When power is turned on, 4-bit operation is automatically selected. One operation is completed in two accesses of 4-bit operation.

(3) 8-bit operation, 8-digit × 2-line display

For 2-line display, the DD RAM address must again be set after the 8th character is completed in the first line (see Table 8).

Note that the first and second lines of the display shift are performed. If shift operation is performed, both the first and second lines move together. When you repeat the shift, the display of the second line will not move to the first line, the same display will only move within each line many times.

Table 6 8-bit Operation, 8-digit × 1-line Display

Instruction	Display	Operation
Power ON and automatic reset		Initialized. No display appears.
Function set 0 0 0 0 1 1 0 * * * RS R/W DB7 ~ DB0		Sets to 8-bit operation and selects 1-line display line. This operation is necessary three times at 100 ms intervals.
Display ON/OFF control 0 0 0 0 0 0 1 1 * *		Display ON. No display appears.
Write data to DD RAM 1 0 0 1 0 0 1 0 0 0	H	Writes "H".
Write data to DD RAM 1 0 0 1 0 0 1 0 0 1	H I	Writes "I".
⋮	⋮	
Write data to DD RAM 1 0 0 1 0 0 1 0 0 1	H I T A C H I	Writes "I".
Write data to DD RAM 1 0 0 0 1 0 0 0 0 0	H I T A C H I	Writes space.
Write data to DD RAM 1 0 0 1 0 0 1 1 0 1	H I T A C H I M	Writes "M", but "M" can't be seen.
Display shift 0 0 0 0 0 1 1 0 * *	I T A C H I M	Shifts left, "M" appears.
⋮	⋮	
Write data to DD RAM 1 0 0 1 0 0 1 1 1 1	I M I C R O K	Writes "O", but "O" can't be seen.
Display shift 0 0 0 0 0 1 1 0 * *	M I C R O K O	Shifts left, "O" appears.
Set DD RAM address 0 0 1 0 0 0 1 1 0 1	M I C R O K O	Writes the address of "K".
Write data to DD RAM 1 0 0 1 0 0 0 0 1 1	M I C R O C O	Changes "K" to "C".

Instruction	Display	Operation
Set DD RAM address 0 0 1 0 0 0 1 1 1 1	M I C R O C O	Writes the address of next to "O".
Write data to DD RAM 1 0 0 1 0 0 1 1 0 1	M I C R O C O	Writes "M", but "M" can't be seen.
Display shift 0 0 0 0 0 1 1 0 * *	M I C R O C O M	Shifts left, "M" appears.
⋮	⋮	
Return home 0 0 0 0 0 0 0 0 1 0	H I T A C H I	Returns both display and DD RAM address to the original position.

Table 7 4-bit Operation, 8-digit × 1-line Display

Instruction	Display	Operation
Power ON and automatic reset		Initialized. No display appears.
Display ON/OFF control RS R/W DB7 ~ DB4 0 0 0 0 0 0 0 0 1 1 * *		Display ON. No display appears.
Write data to DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H	Writes "H".
Hereafter, control is the same as 8-bit operation.		

Table 8 8-bit Operation, 8-digit × 2 lines Display

Instruction	Display	Operation
Power on and automatic reset		Initialized. No display appears.
Function set 0 0 0 0 1 1 * * * * RS R/W DB7 ~ DB0		This instruction is necessary three times at 100 ms intervals.
Function set 0 0 0 0 1 1 1 * * * RS R/W DB7 ~ DB0		Sets 8-bit operation and 2-line display.
Display ON/OFF control 0 0 0 0 0 0 1 1 * *		Display ON. No display appears.
Write data to DD RAM 1 0 0 1 0 0 1 0 0 1	H	Write "H".
⋮	⋮	
Write data to DD RAM 1 0 0 1 0 0 1 0 0 1	H I T A C H I	Writes "I".
Set DD RAM address 0 0 1 0 0 1 0 0 0 0	H I T A C H I	Sets DD RAM address to the top of the second line.
Write data to DD RAM 1 0 0 1 0 0 1 1 0 1	H I T A C H I M	Writes "M".
⋮	⋮	
Write data to DD RAM 1 0 0 1 0 0 1 1 1 1	H I T A C H I M I C R O C O	Writes "O".
Write data to DD RAM 1 0 0 1 0 0 1 1 0 1	H I T A C H I M I C R O C O M	Writes "M".
Display shift 0 0 0 0 0 1 1 0 * *	I T A C H I I C R O C O M	Shifts left. Both line will be shifted.
Return home 0 0 0 0 0 0 0 0 1 *	H I T A C H I M I C R O C O M	Returns display to the original position.

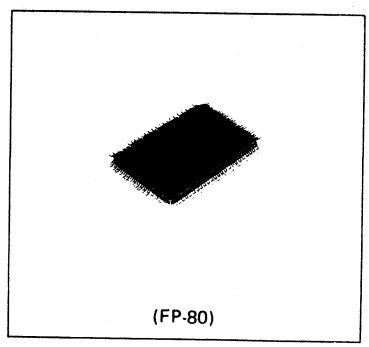
HD44102CH (DOT MATRIX LIQUID CRYSTAL GRAPHIC DISPLAY COLUMN DRIVER)

The HD44102CH is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit microcomputer in the internal display RAM and generating dot matrix liquid crystal driving signals.

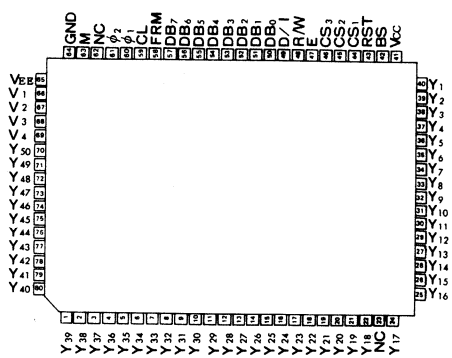
Each bit data of display RAM corresponds to ON/OFF of each dot of liquid crystal display to provide more flexible display.

The HD44102CH is produced in the CMOS process. Therefore, the combination with a CMOS microcomputer can accomplish a portable battery drive equipment utilizing the liquid crystal display's lower power dissipation.

The combination of HD44102CH with the row (common) driver HD44103CH facilitates dot matrix liquid crystal graphic display system configuration.



PIN ARRANGEMENT

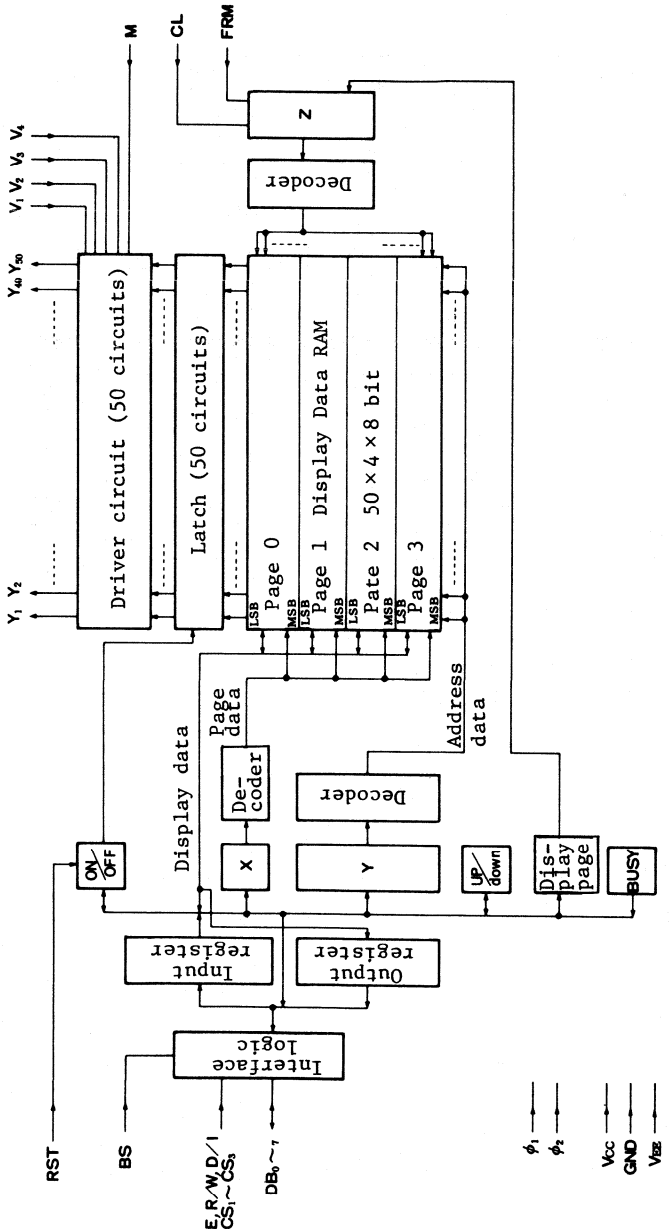


(TOP VIEW)

■ FEATURES

- Dot matrix liquid crystal graphic display column driver incorporating display RAM.
- Interfaceable to 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  RAM bit data "1" ..... ON
  RAM bit data "0" ..... OFF
- Display RAM capacity ..... 50 × 8 × 4 (1600 bits)
- Internal liquid crystal display driver circuit (segment output) .....
  50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  Selectable duty factors 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  Display Data, Read/Write, Display ON/OFF, Set Address, Set Display Start Page, Set UP/DOWN, Read Status
- Low power dissipation
- Power supplies ..... V_{CC} 5V±10%, V_{EE} 0∿-5V
- CMOS process
- 80-pin flat plastic package

■BLOCK DIAGRAM



■TABLE OF PIN ASSIGNMENT

No.	Power supply, Clock	Input	Output	No.	Power supply, Clock	Input	Output
1			Y39	41	V_{CC}		
2			Y38	42		BS	
3			Y37	43		RST	
4			Y36	44		CS1	
5			Y35	45		CS2	
6			Y34	46		CS3	
7			Y33	47		E	
8			Y32	48		R/W	
9			Y31	49		D/I	
10			Y30	50		DB_0	DB_0
11			Y29	51		DB_1	DB_1
12			Y28	52		DB_2	DB_2
13			Y27	53		DB_3	DB_3
14			Y26	54		DB_4	DB_4
15			Y25	55		DB_5	DB_5
16			Y24	56		DB_6	DB_6
17			Y23	57		DB_7	DB_7
18			Y22	58		FRM	
19			Y21	59		CL	
20			Y20	60	ϕ_1		
21			Y19	61	ϕ_2		
22			Y18	62		N. C.	
23		N. C.		63		M	
24			Y17	64	GND		
25			Y16	65	V_{EE}		
26			Y15	66	V_1		
27			Y14	67	V_2		
28			Y13	68	V_3		
29			Y12	69	V_4		
30			Y11	70			Y50
31			Y10	71			Y49
32			Y9	72			Y48
33			Y8	73			Y47
34			Y7	74			Y46
35			Y6	75			Y45
36			Y5	76			Y44
37			Y4	77			Y43
38			Y3	78			Y42
39			Y2	79			Y41
40			Y1	80			Y40

(Note) N.C.: Nonconnection pin

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	(1)
Supply voltage (2)	V_{EE}	V_{CC}-13.5 ∿ V_{CC}+0.3	V	
Input voltage (1)	V_{T1}	-0.3 ∿ V_{CC}+0.3	V	(1)(2)
Input voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC}+0.3	V	(3)
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: Referenced to GND=0.

Note 2: Applied to input terminals (except V1, V2, V3 and V4), and I/O common terminals.

Note 3: Applied to terminals V1, V2, V3 and V4.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, GND=0V, V_{EE}=0∿-5.5V, Ta=-20∿+75°C) (Note 4)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "High" voltage(CMOS)	V_{IHC}		0.7×V_{CC}	-	V_{CC}	V	5
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3×V_{CC}	V	5
Input "High" voltage (TTL)	V_{IHT}		2.0	-	V_{CC}	V	6
Input "Low" voltage (TTL)	V_{ILT}		0	-	+0.8	V	6
Output "High" voltage	V_{OH}	I_{OH}=-250μA	+3.5	-	-	V	7
Output "Low" voltage	V_{OL}	I_{OL}=+1.6mA	-	-	+0.4	V	7
Xi-Xj ON resistance	R_{ON}	V_{EE}=-5V±10%, Load current 100μA	-	-	7.5	kΩ	
Input leakage current (1)	I_{IL1}	V_{IN}=V_{CC}∿GND	-1	-	1	μA	8
Input leakage current (2)	I_{IL2}	V_{IN}=V_{CC}∿V_{EE}	-2	-	2	μA	9
Operating frequency	F_{CLK}	φ1 φ2 frequency	25	-	250	kHz	10
Dissipation current (1)	I_{CC1}	F_{clk}=200kHz frame= 65Hz during display	-	-	100	μA	11
Dissipation current (2)	I_{CC2}	Access cycle 1MHz at access	-	-	500	μA	12

Note 4: Specified within this range unless otherwise noted.

Note 5: Applied to M, FRM, CL, BS, RST, $\phi 1$, $\phi 2$.

Note 6: Applied to CS1 to CS3, E, D/I, R/W and DB0 to DB7.

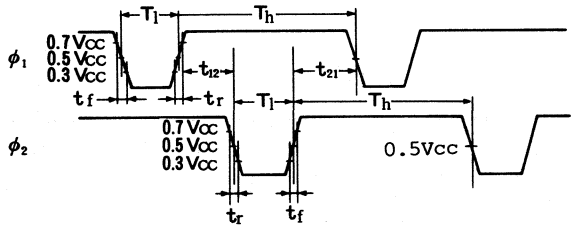
Note 7: Applied to DB0 to DB7.

Note 8: Applied to input terminals, M, FRM, CL, BS, RST, $\phi 1$, $\phi 2$, CS1 to CS3, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.

Note 9: Applied to V1, V2, V3 and V4.

Note 10: $\phi 1$ and $\phi 2$ AC characteristics.

	Symbol	Min.	Typ	Max.	Unit
Duty	Duty	20	25	30	%
Fall time	t_f	-	-	100	ns
Rise time	t_r	-	-	100	ns
Phase difference time	t_{12}	0.8	-	-	µs
Phase difference time	t_{21}	0.8	-	-	µs
$T_l + T_h$		-	-	40	µs



$$F_{CLK} = \frac{1}{T_l + T_h}$$

$$D_{uty} = \frac{T_l}{T_l + T_h} \times 100\ (\%)$$

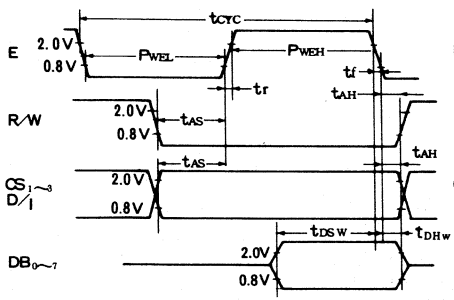
Note 11: Measured by V_{CC} terminal at no output load, at 1/32 duty, and frame frequency of 65Hz, in checker pattern display. Access from the CPU is stopping.

Note 12: Measured by V_{CC} terminal at no output load, 1/32 duty and frame frequency of 65Hz.

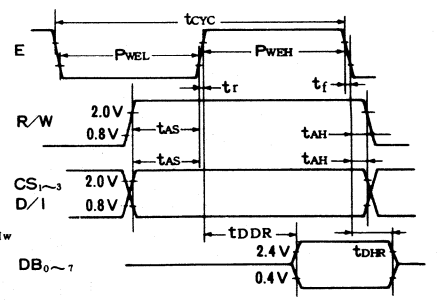
●INTERFACE AC CHARACTERISTICS

Item	Symbol	Min.	Typ	Max.	Unit	Note
E cycle time	t_{CYC}	1000	-	-	ns	13, 14
E high level width	PWEH	450	-	-	ns	13, 14
E low level width	PWEL	450	-	-	ns	13, 14
E rise time	t_r	-	-	25	ns	13, 14
E fall time	t_f	-	-	25	ns	13, 14
Address setup time	t_{AS}	140	-	-	ns	13, 14
Address hold time	t_{AH}	10	-	-	ns	13, 14
Data setup time	t_{DSW}	200	-	-	ns	13
Data delay time	t_{DDR}	-	-	320	ns	14, 15
Data hold time at write	t_{DHW}	10	-	-	ns	13
Data hold time at read	t_{DHR}	20	-	-	ns	14

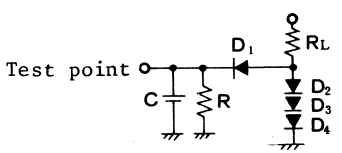
Note 13: At CPU write



Note 14: At CPU read



Note 15: DB0 to DB7 load circuits



R_L = 2.4kΩ

R = 11kΩ

C = 130pF (including jig capacity)

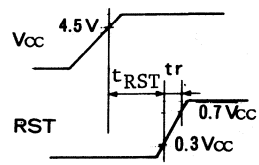
Diodes D1 to D4 are all 1S2074 Ⓗ

Note 16: Display OFF at initial power up.

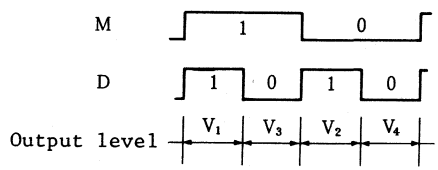
The HD44102CH can be placed in the display OFF state by setting terminal RST to "LOW" at initial power up.

No instruction other than the Read Status cannot be accepted while the RST is in the "Low" level.

		Min.	Typ	Max.	Unit
Reset time	t_{RST}	1.0	-	-	μs
Rise time	t_r	-	-	200	ns



■ TERMINAL FUNCTIONS DESCRIPTION

Signal name	Number of terminals	I/O	Function
Y1∿Y50	50	O	Liquid crystal display drive output. Relationship among output level, M and display data (D): 
CS1∿CS3	3	I	Chip select CS1 CS2 CS3 State L L L Non-selected L L H Non-selected L H L Non-selected L H H Selected read/write enable H L L Selected write enable only H L H Selected write enable only H H L Selected write enable only H H H Selected read/write enable
E	1	I	Enable At write (R/W=L): Data of DB0 to DB7 is latched at the fall of E. At read (R/W=H): Data appears at DB0 to DB7 while E is in "High" level.

<table>
<tr><th>Signal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>R/W</td><td>1</td><td>I</td><td>Read/Write
R/W=H: Data appears at DB0 to DB7 and can be read by the CPU when E=H and CS2/CS3="H".
R/W=L: DB0 to DB7 can accept input when CS2/CS3=H or CS1=H.</td></tr>
<tr><td>D/I</td><td>1</td><td>I</td><td>Data/Instruction
D/I=H: Indicates that the data of DB0 to DB7 is display data.
D/I=L: Indicates that the data of BD0 to DB7 is display control data.</td></tr>
<tr><td>DB0∿DB7</td><td>8</td><td>I/O</td><td>Data bus, Three-state I/O common terminal
<table>
<tr><th>E</th><th>R/W</th><th>CS1</th><th>CS2</th><th>CS3</th><th>State of DB0 to DB7</th></tr>
<tr><td>H</td><td>H</td><td>*</td><td>H</td><td>H</td><td>Output state</td></tr>
<tr><td>*</td><td>L</td><td>H</td><td>*</td><td>*</td><td rowspan="2">Input state,
High impedance</td></tr>
<tr><td>*</td><td>L</td><td>*</td><td>H</td><td>H</td></tr>
<tr><td colspan="5">Others</td><td>High impedance</td></tr>
</table></td></tr>
<tr><td>M</td><td>1</td><td>I</td><td>Signal to convert liquid crystal display drive output to AC</td></tr>
<tr><td>CL</td><td>1</td><td>I</td><td>Display synchronous signal
At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.</td></tr>
<tr><td>FRM</td><td>1</td><td>I</td><td>Display synchronous signal (frame signal)
This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.</td></tr>
<tr><td>ϕ1, ϕ2</td><td>2</td><td>I</td><td>2-phase clock signal for internal operation
The ϕ1 and ϕ2 clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.</td></tr>
<tr><td>RST</td><td>1</td><td>I</td><td>Reset signal
The display disappears and Y address counter is set in the UP counter state by setting the RST signal to "Low" level. After releasing reset, the display OFF state and up mode is held until the state is changed by the instruction.</td></tr>
<tr><td>BS</td><td>1</td><td>I</td><td>Bus select signal
BS=L: DB0 to DB7 operate in 8-bit length.
BS=H: DB4 to DB7 are valid in 4-bit length only. 8-bit data is accessed twice in the high and low order.</td></tr>
</table>

Signal name	Number of terminals	I/O	Function
V1,V2, V3,V4	4		Power supply for liquid crystal display drive. V1 and V2: Selection voltage V3 and V4: Non-selection voltage
V_{CC} GND V_{EE}	3		Power supply. V_{CC}-GND: Power supply for internal logic V_{CC}-V_{EE}: Power supply for liquid crystal display drive circuit logic

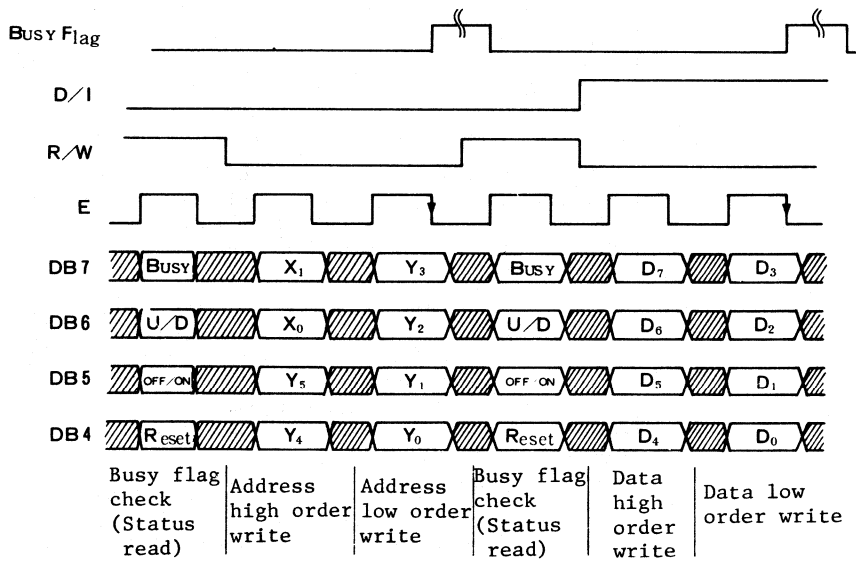
■FUNCTION OF EACH BLOCK

●Interface Logic

The HD44102CH can use the data bus in 4-bit or 8-bit word length to enable the interface to a 4-bit or 8-bit CPU.

(1) 4-bit mode (BS=H)

8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high. The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) is transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).



(Note) Execute the instructions other than Status Read in 4-bit length each. The busy flag is set at the fall of the second E signal. The Status Read is executed once. After the execution of the Status Read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

(2) 8-bit mode (BS=L)

If the BS signal is low, the 8 data buses (DB0 to DB7) are used for data transfer.

DB7 ... MSB (Most significant bit)

DB0 ... LSB (Least significant bit)

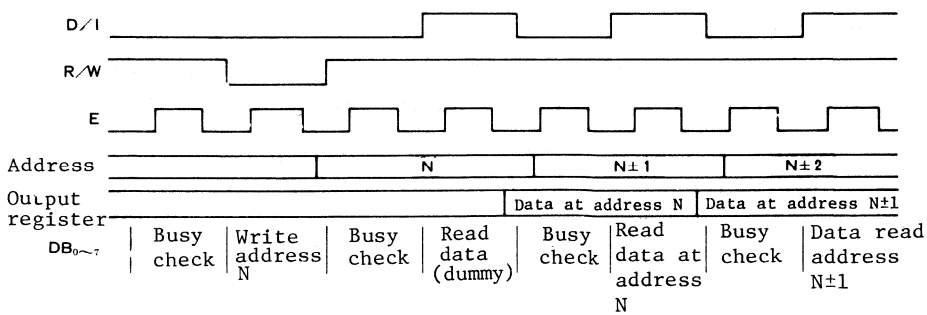
For AC timing, refer to (Note 12) to (Note 15) of "ELECTRICAL CHARACTERISTICS".

● Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of E signal when the CS is in the select state and R/W is write state.

● Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data.



● X,Y Address Counter

The X,Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit UP/DOWN counter. The address is increased or decreased by 1 by the read/write operation of display data. The UP/DOWN mode can be determined by the instruction or RST signal. The Y address register loops the values of 0 to 49 to count. The X address register has no count function.

●Display ON/OFF Flip Flop

This flip flop is set to ON/OFF state by the instruction or RST signal. In the OFF state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the ON state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display ON/OFF.

●UP/DOWN Flip Flop

This flip flop determines the count mode of the Y address counter. In the UP mode, the Y address register is increased by 1. 0 follows 49. In the DOWN mode, the register is decreased by 1. 0 is followed by 49.

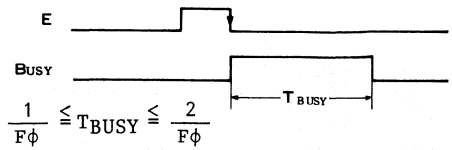
● Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

●Busy Flag

After the instruction other than Status Read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective. The value can be read out on DB7 by the Status Read instruction.

The HD44102CH cannot accept any other instructions than the Status Read in the busy state. Make sure the busy flag is reset before the issue of instruction.



$$\frac{1}{F\phi} \leqq T_{BUSY} \leqq \frac{2}{F\phi}$$

Fϕ is ϕ1, ϕ2 frequency (half of HD44103CH oscillation frequency)

● Z Address Counter

The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputing the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

● Latch

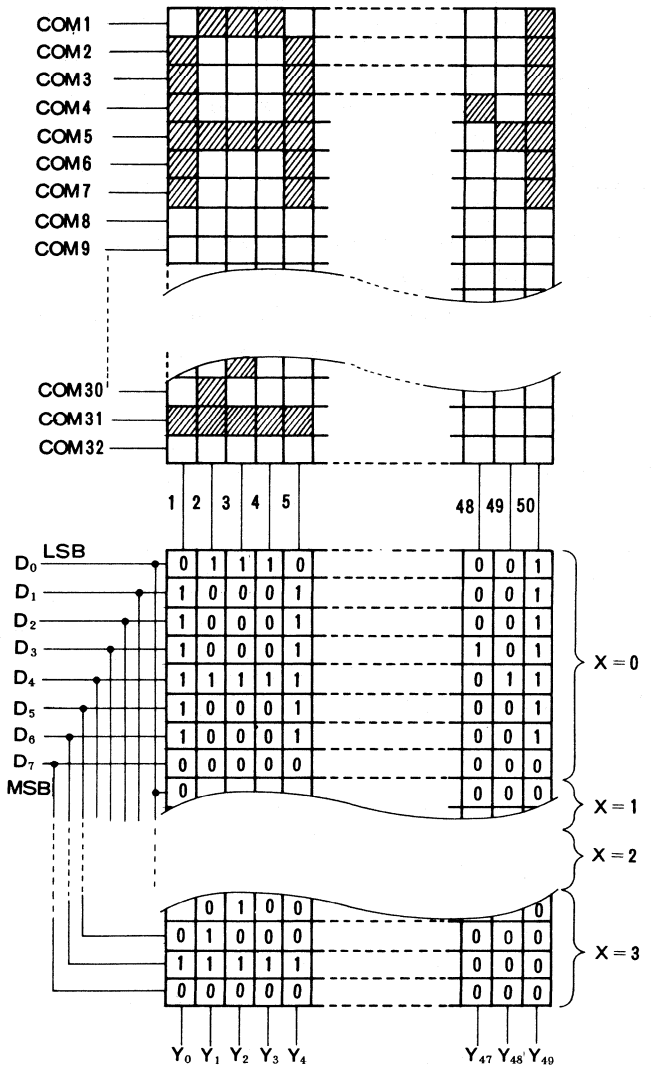
The display data from the display data RAM is latched at the rise of CL signal.

● Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of latched display data and M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.

● Display RAM

Relationship between Data in RAM and Display
(Display start page 0, 1/32 duty)



Display pattern

Data in display RAM

■DISPLAY CONTROL INSTRUCTIONS

(1) Read/Write Display Data

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
1	1	(Display data)								Read (CPU ← HD44102CH)
0	1	(Display data)								Write (CPU → HD44102CH)

Sends or receives data to or from the address of the display RAM specified in advance. However, the dummy read may be required for reading display data. Refer to the description of the output register in the FUNCTION OF EACH BLOCK.

(2) Display ON/OFF

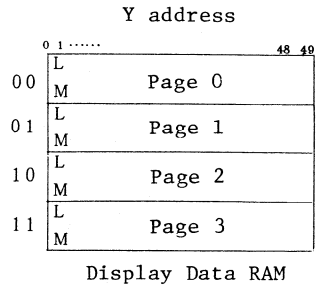
		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	0	1	Display ON
0	0	0	0	1	1	1	0	0	0	Display OFF

Controls the ON/OFF of display. RAM data is not affected.

(3) Set X/Y Address

		MSB			DB				LSB
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0						
0	0	0	1	Binary numbers of 0∿49					
0	0	1	0						
0	0	1	1						

X address (page) — Y address (address)



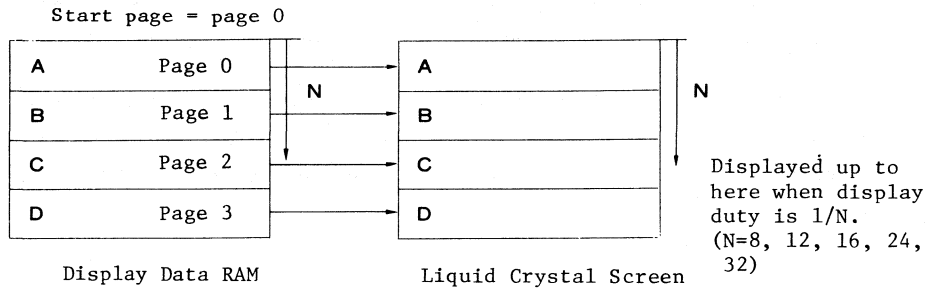
(4) Display Start Page

		MSB			DB				LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	1	1	0	..... Refer to Fig. A.
0	0	0	1	1	1	1	1	1	0	..... Refer to Fig. B.
0	0	1	0	1	1	1	1	1	0	..... Refer to Fig. C.
0	0	1	1	1	1	1	1	1	0	..... Refer to Fig. D.

Display start page

Specifies a RAM page displayed at the top of the screen. Display is as shown in Figs. A, B, C and D respectively. When the display duty is more than 1/32 (For example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

Fig. A



Displayed up to here when display duty is 1/N. (N=8, 12, 16, 24, 32)

Fig. B

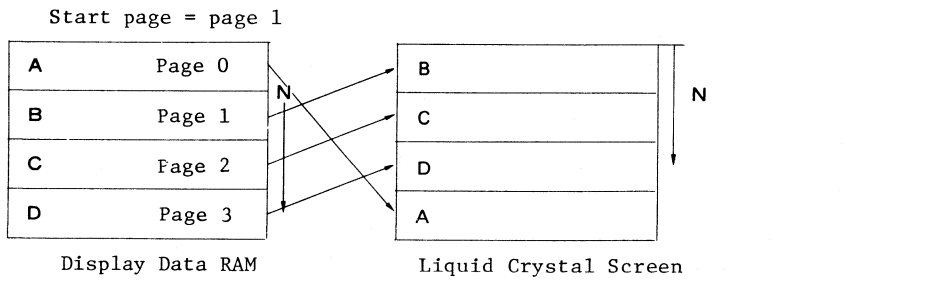


Fig. C

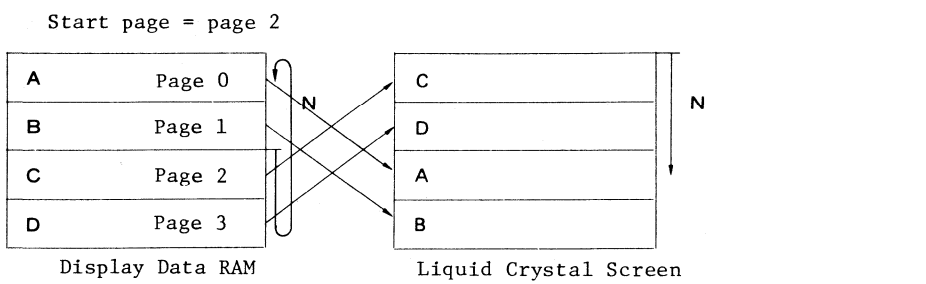
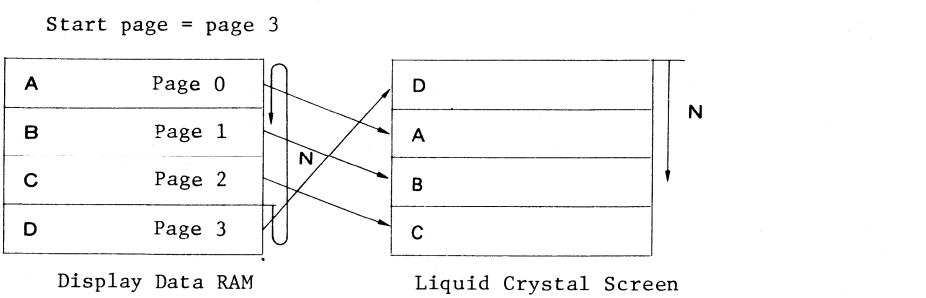


Fig. D



(5) UP/DOWN Set

R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	1	1	UP mode
0	0	0	0	1	1	1	0	1	0	DOWN mode

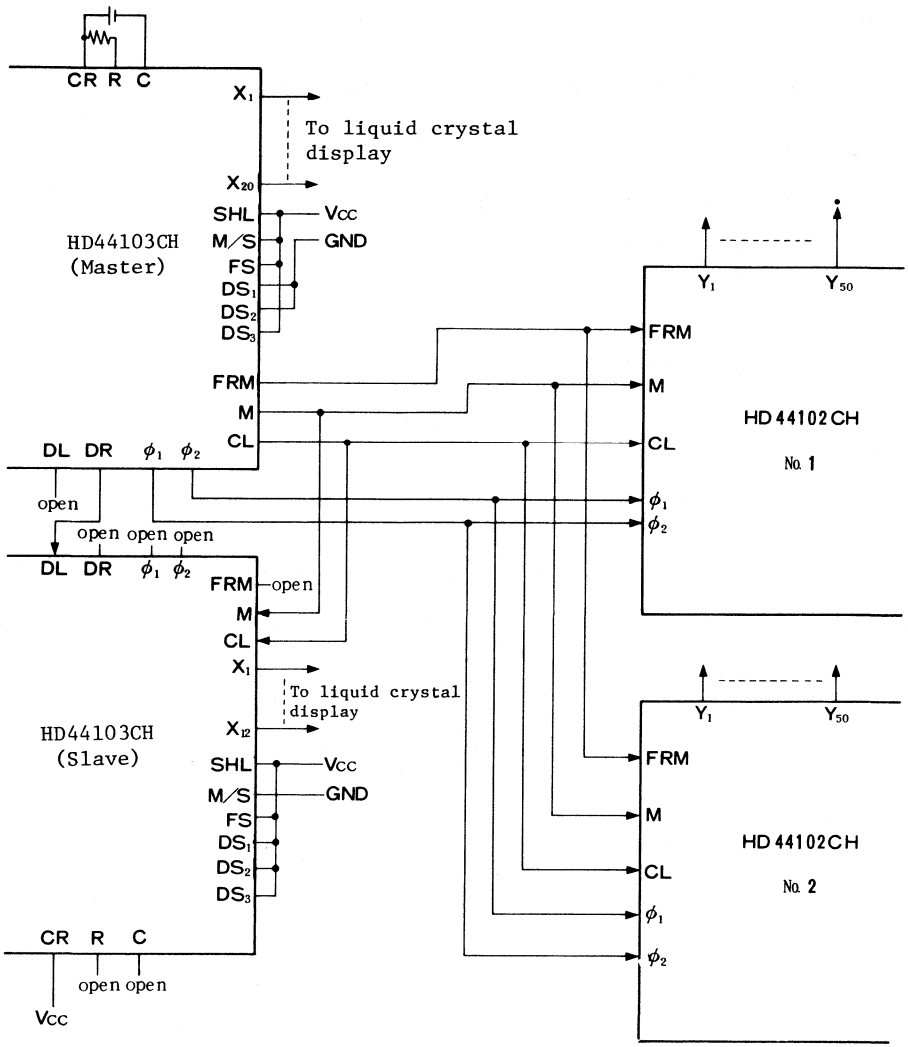
Sets Y address register in the UP/DOWN counter mode.

(6) Status Read

R/W	D/I	7	6	5	4	3	2	1	0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0

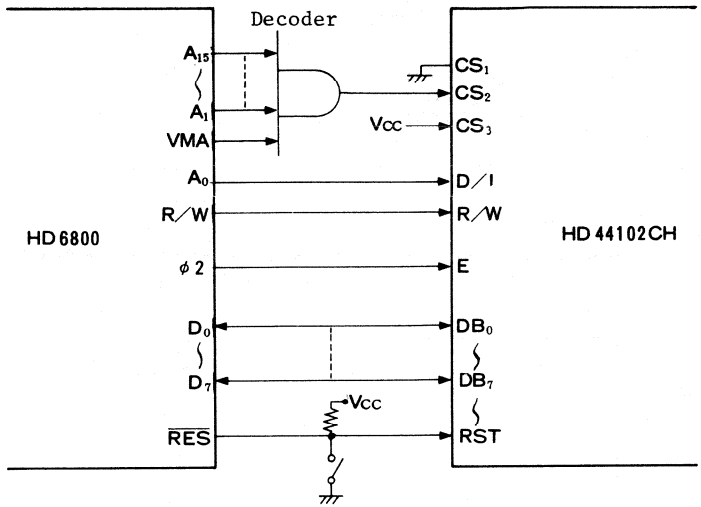
- RESET → Goes to "1" when RST is in the reset state (Busy also goes to "1").
  Goes to "0" when RST is in the operating state.
- OFF/ON → Goes to "1" in the display OFF state.
  Goes to "0" on the display ON state.
- UP/DOWN → Goes to "1" when address counter is in the UP mode.
  Goes to "0" when address counter is in the DOWN mode.
- BUSY → Goes to "1" while instructions (1) ∿ (5) are being executed.
  During "1", none of instructions (1) ∿ (5) are accepted.

■CONNECTION BETWEEN LCD DRIVERS (EXAMPLE OF 1/32 DUTY)



■INTERFACE TO CPU

(1) Example of connection to HD6800



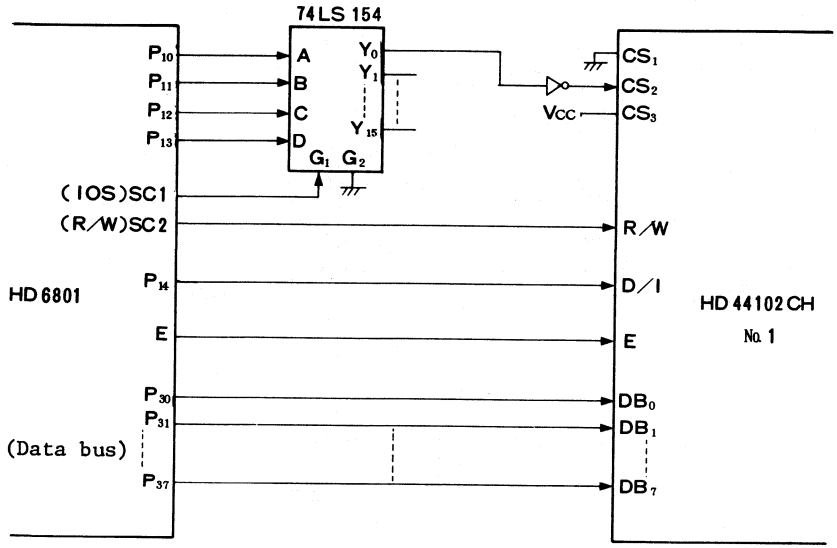
Example of Connection to HD6800 Series

In the decoder given in this example, the addresses of HD44102CH in the address space of HD6800 are:

Read/write of display data : $'FFFF'
Write of display instruction: $'FFFE'
Read of status : $'FFFE'

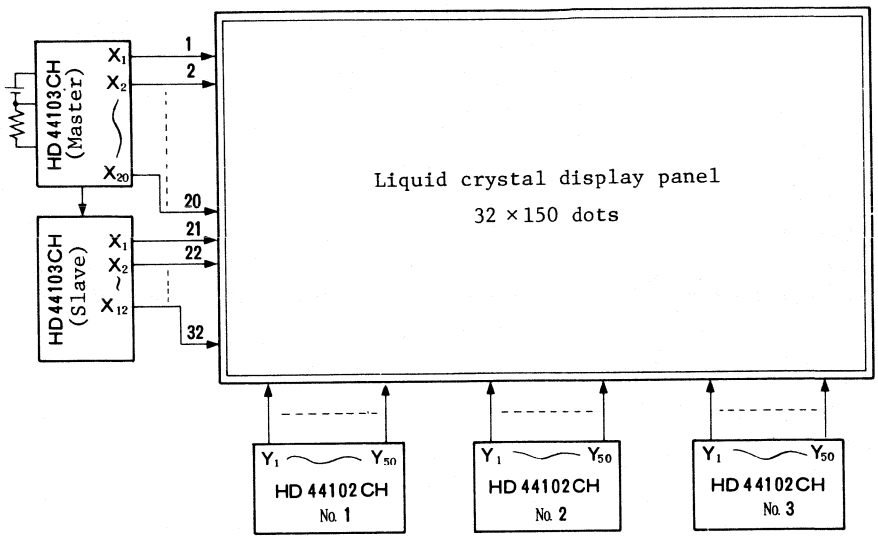
Thus, the HD44102CH can be controlled by reading/writing data at these addresses.

(2) Example of connection to HD6801

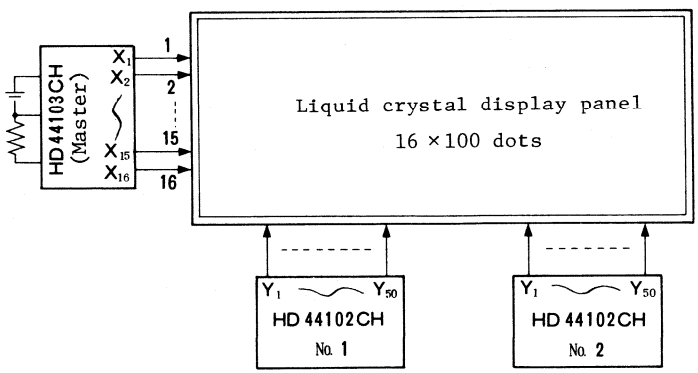


- The HD6801 is set to mode 5. P10 ∿P14 are used as output ports, and P30 ∿P37 are used as data buses.
- The 74LS154 is a 4-to-16 decoder that decodes 4 bits of P10 ∿P13 to select the chips.
- Therefore, the HD44102CH can be controlled by selecting the chips through P10 ∿P13 and specifying the D/I signal through P14 in advance, and later conducting memory Read or Write for external memory space ($0100 to $01FF) of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to each manual.

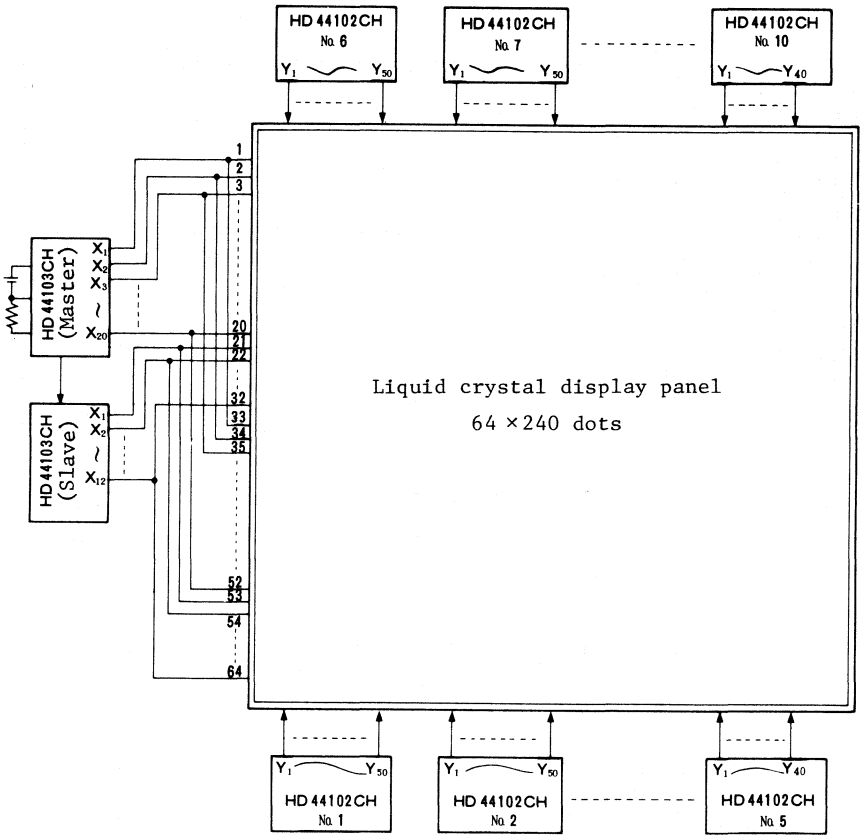
■CONNECTION TO LIQUID CRYSTAL DISPLAY



(a) Example of connection of 1/32 duty, 1-screen display



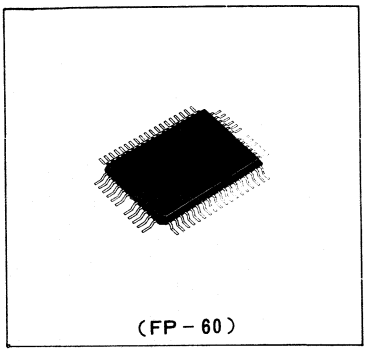
(b) Example of connection of 1/16 duty, 1-screen display



(c) Example of connection of 1/32 duty, 2-screen display

HD44103CH (DOT MATRIX LIQUID CRYSTAL GRAPHIC DISPLAY COMMON DRIVER)

The HD44103CH is a common signal driver for dot matrix liquid crystal graphic display systems. It generates the timing signals required for display with its internal oscillator and supplies them to the column driver (HD44102CH) to control display, also automatically scanning the common signals of the liquid crystal according to the display duty. It can select 5 types of display duties ratio: 1/8, 1/12, 1/16, 1/24 and 1/32. 20 driver output lines are provided, and the impedance is low (500Ω max.) to enable a large screen to be driven.

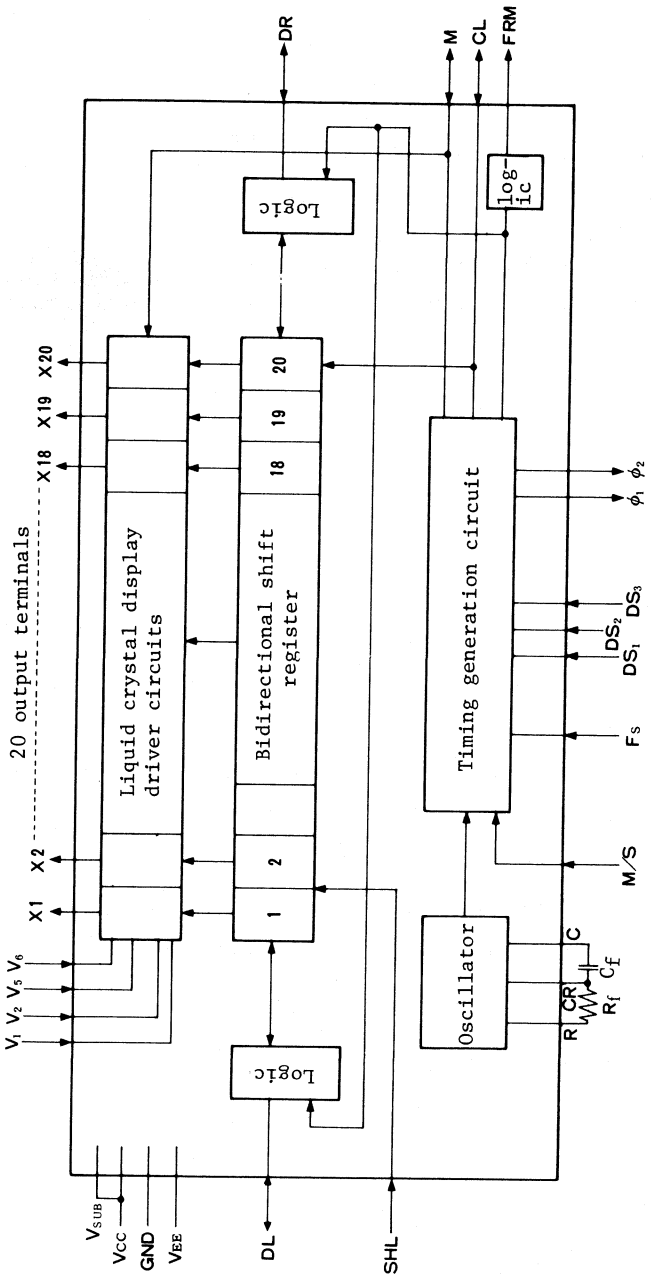


(FP-60)

■ FEATURES

- Dot matrix liquid crystal graphic display common driver incorporating the timing generation circuit in it.
- Internal oscillator (Oscillation frequency can be selected by attaching an oscillation resistor and an oscillation capacity)
- Generates display timing signals.
- 20-bit bidirectional shift register for generating common signals
- 20 liquid crystal driver circuits with low output impedance
- Selectable display duty ratio: 1/8, 1/12, 1/16, 1/24, 1/32
- Low power dissipation
- Power supplies: V_{CC} ... +5V±10%, V_{EE} ... 0 to -5.5V
- CMOS process
- 60-pin plastic flat package

■BLOCK DIAGRAM



● TERMINAL ARRANGEMENT LIST

No.	Power supply, Clock	Input	Output	No.	Power supply, Clock	Input	Output
1			X 14	31	CR		
2			X 13	32			ϕ_1
3			X 12	33			ϕ_2
4			X 11	34	GND		
5			X 10	35		FS	
6			X 9	36		DS1	
7	N. C.			37	N. C.		
8			X 8	38	N. C.		
9			X 7	39	N. C.		
10			X 6	40		DS2	
11			X 5	41		DS3	
12	N. C.			42		M	M
13	N. C.			43			FRM
14	N. C.			44		SHL	
15	N. C.			45	Vcc		
16			X 4	46	N. C.		
17			X 3	47	N. C.		
18			X 2	48	N. C.		
19			X 1	49		M/S	
20	V_1			50		CL	CL
21	N. C.			51	N. C.		
22	N. C.			52	N. C.		
23	V_2			53	N. C.		
24	V_5			54		DR	DR
25	V_6			55			X 20
26	V_{EE}			56			X 19
27		DL	DL	57			X 18
28	C			58			X 17
29	V_{SUB}	Connect to V_{CC}.		59			X 16
30	R			60			X 15

(Note) N.C.: Unused terminal
Connect V_{SUB} to V_{CC}.

● ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rated value	Unit	Note
Supply voltage (1)	V_{CC}	-0.3 ∿ +7.0	V	(1)
Supply voltage (2)	V_{EE}	V_{CC}-13.5 ∿ V_{CC}+0.3	V	(14)
Terminal voltage (1)	V_{T1}	-0.3 ∿ V_{CC}+0.3	V	(1), (2)
Terminal voltage (2)	V_{T2}	V_{EE}-0.3 ∿ V_{CC}+0.3	V	(3)
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: Referenced to GND=0.

Note 2: Applied to input terminals and I/O common terminals except V1, V2, V3 and V4.

Note 3: Applied to terminals V1, V2, V3 and V4.

Note 14: Connect a protection resistor of 220Ω±5% to V_{EE} power supply in series.

● ELECTRICAL CHARACTERISTICS

(V_{CC}=+5V±10%, GND=0V, V_{EE}=0 to -5.5V, Ta=-20 to +75°C) (Note 4)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "high" voltage	V_{IH}		0.7×V_{CC}	-	V_{CC}	V	(5)
Input "low" voltage	V_{IL}		0	-	0.3×V_{CC}	V	(5)
Output "high" voltage	V_{OH}	I_{OH}=-400μA	V_{CC}-0.4	-	-	V	(6)
Output "low" voltage	V_{OL}	I_{OL}=+400μA	-	-	0.4	V	(6)
Vi-Xj ON resistance	R_{ON}	V_{EE}=-5V±10%, Load current ±150μA	-	-	500	Ω	
Input leakage current (1)	I_{IL1}	V_{IN}=V_{CC}∿GND	-1	-	1	μA	(7)
Input leakage current (2)	I_{IL2}	V_{IN}=V_{CC}∿V_{EE}	-2	-	2	μA	(8)
Shift frequency	f_{SFT}	In slave mode	-	-	50	kHz	(9)
Oscillation frequency	f_{OSC}	R_f=70kΩ2%, C_f=10pF±5%	300	430	560	kHz	(10)
External clock operating frequency	f_{cp}		50	-	560	kHz	
External clock duty	Duty		45	50	55	%	(11)
External clock rise time	t_{rcp}		-	-	50	ns	(11)
External clock fall time	t_{fcp}		-	-	50	ns	(11)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Dissipation current (master)	P_{w1}	CR oscillation= 430kHz	-	-	4.4	mW	(12)
Dissipation current (slave)	P_{w2}	Frame frequency =70Hz	-	-	1.1	mW	(13)

Note 4: Specified within this range unless otherwise noted.

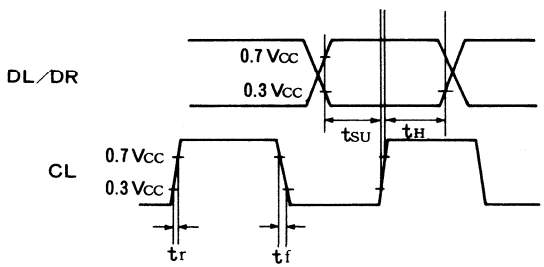
Note 5: Applied to CR, FS, DS1 to DS3, M, SHL, M/S, CL, DR and DL.

Note 6: Applied to DL, DR, M, FRM, CL, $\phi 1$ and $\phi 2$.

Note 7: Applied to input terminals CR, FS, DS1 to DS3, SHL and M/S, and I/O common terminals DL, DR, M and CL at high impedance.

Note 8: Applied to V1, V2, V5 and V6.

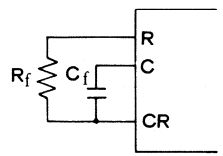
Note 9: Shift operation timing



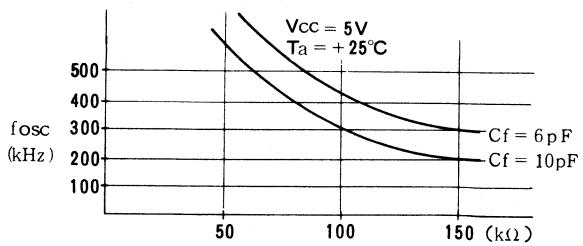
	min	typ	max	unit
t_{SU}	5	–	–	μs
t_H	5	–	–	μs
t_r	–	–	100	ns
t_f	–	–	100	ns

Note 10: Relationship between oscillation frequency and R_f/C_f

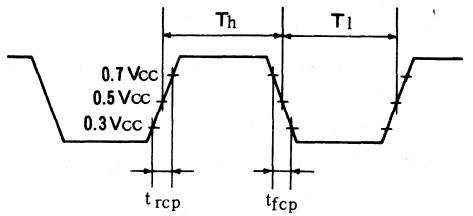
CR oscillator



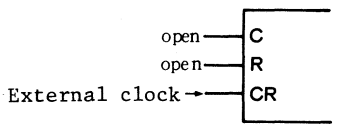
The values of Rf and Cf are typical values. The oscillation frequency varies with the mounting condition. Adjust oscillation frequency to a required value.



Note 11:



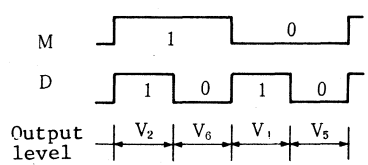
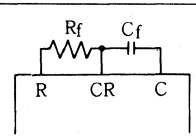
$$Duty = \frac{Th}{Th + Tl}$$



Note 12: Measured by V_{CC} terminal at output non-load of R_f=70kΩ±2% and C_f=10pF±5%, 1/32 duty in the master mode.

Note 13: Measured by V_{CC} terminal at output non-load, 1/32 duty, frame frequency of 70Hz in the slave mode.

● TERMINAL FUNCTIONS

Terminal name	Number of terminals	I/O	Function
X1∿X20	20	O	Liquid crystal display driver output. Relationship among output level, M and data (D) in shift register. 
CR, R, C	3		Oscillator  CR oscillator
M	1	I/O	Signal for converting liquid crystal display driver signal into AC Master: Output terminal Slave : Input terminal

<table>
<tr><th>Terminal name</th><th>Number of terminals</th><th>I/O</th><th>Function</th></tr>
<tr><td>CL</td><td>1</td><td>I/O</td><td>Shift register shift clock.
Master: Output terminal
Slave : Input terminal</td></tr>
<tr><td>FRM</td><td>1</td><td>O</td><td>Frame signal, Display synchronous signal</td></tr>
<tr><td>DS1∿DS3</td><td>3</td><td>I</td><td>Display duty ratio select.
<table>
<tr><td>Display duty ratio</td><td>1/24</td><td colspan="2">1/12</td><td>X</td><td>1/32</td><td colspan="2">1/16</td><td>1/8</td></tr>
<tr><td>DS1</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td>FS</td><td>1</td><td>I</td><td>Frequency select.
The relationship between the frame frequency f_{FRM} and the oscillation frequency f_{OSC} is as follows:
FS="H": $f_{OSC} = 6144 \times f_{FPM}$ ... (1)
FS="L": $f_{OSC} = 3072 \times f_{FRM}$ ... (2)
Example 1) When FS="H", adjust Rf and Cf so that the oscillation frequency is approx. 430kHz if the frame frequency is 70Hz.
Example 2) When FS="L", adjust Rf and Cf so that the oscillation is approx. 215kHz, in order to obtain the same display waveforms as Example 1. When compared with Example 1, the power dissipation is reduced because of the operation at lower frequency. However, the operating clocks $\phi 1$ and $\phi 2$ supplied to the column driver have lower frequencies. Therefore, the access time of the column driver HD44102CH becomes longer.</td></tr>
<tr><td>DL, DR</td><td>2</td><td>I/O</td><td>Data I/O terminals of bidirectional shift register.</td></tr>
<tr><td>SHL</td><td>1</td><td>I</td><td>Shift direction select of bidirectional shift register.
<table>
<tr><td>SHL</td><td>Shift direction</td></tr>
<tr><td>H</td><td>DL → DR</td></tr>
<tr><td>L</td><td>DL ← DR</td></tr>
</table></td></tr>
</table>

Terminal name	Number of terminals	I/O	Function
M/S	1	I	Master/slave select. M/S="H": Master mode The oscillator and timing generation circuit operate to supply display timing signals to the display system. Each of I/O common terminals, DL, DR, M and CL is placed in the output state. M/S="L": Slave mode The timing generation circuit stops operating. The oscillator is not required. Connect terminal CR to V_{CC}. Open terminals C and R. One (determined by SHL) of DL and DR, and terminals M and CL are placed in the input state. Connect M, CL and one of DL and DR of the master to the respective terminals. Connect FD, DS1, DS2 and DS3 to V_{CC}. When display duty ratio is 1/8, 1/12 or 1/16, one HD44103CH is required. Use it in the master mode. When display duty ratio is 1/24 or 1/32, two HD44103CHs are required. Use the one in the master mode to drive common signals 1 to 20, and the other in the slave mode to drive common signals 21 to 24 (32).
ϕ1, ϕ2	2	O	Operating clock output terminals for HD44102CH. The frequencies of ϕ1 and ϕ2 become half of oscillation frequency.
V1, V2, V5, V6	4		Liquid crystal display driver level power supply V1 and V2: Selected level V5 and V6: Non-selected level
V_{CC} GND V_{EE}	3		Power supply. V_{CC}-GND: Power supply for internal logic V_{CC}-V_{EE}: Power supply for driver circuit logic

● BLOCK FUNCTIONS

Oscillator

The oscillator is a CR oscillator that attaches an oscillation resistor Rf and oscillation capacity Cf. The oscillation frequency varies with the values of Rf and Cf and the mounting conditions. Refer to ELECTRICAL CHARACTERISTICS (Note 10) to make proper adjustment.

Timing Generation Circuit

The timing generation circuit divides the signals from the oscillator and generates display timing signals (M, CL and FRM) and operating clock (ϕ1 and ϕ2) for HD44102CH according to the display duty ratio set by DS1 to DS3. In the slave mode, this block stops operating. It is meaningless to set FS, DS1 to DS3. However, connect them to V_{CC} to prevent floating current.

Bidirectional Shift Register

This is a 20-bit bidirectional shift register. The shift direction is determined by the SHL. The data input from DL or DR performs a shift operation at the rise of shift clock CL.

Liquid Crystal Display Driver Circuit

Each of 20 driver circuits is a multiplex circuit composed of four CMOS switches. The combination of the data from the shift register with M signal allows one of the four liquid crystal display driver levels V1, V2, V5 and V6 to be transferred to the output terminals.

● APPLICATIONS

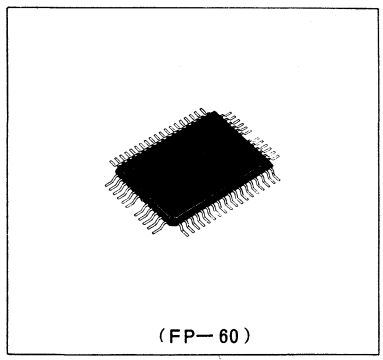
Refer to the applications of the HD44102CH.

HD61830 (DOT MATRIX LIQUID CRYSTAL GRAPHIC DISPLAY CONTROLLER)

The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

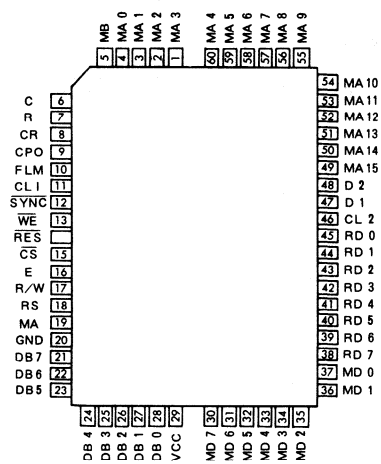
It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

The HD61830 is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power dissipation.



(FP—60)

■ PIN ARRANGEMENT

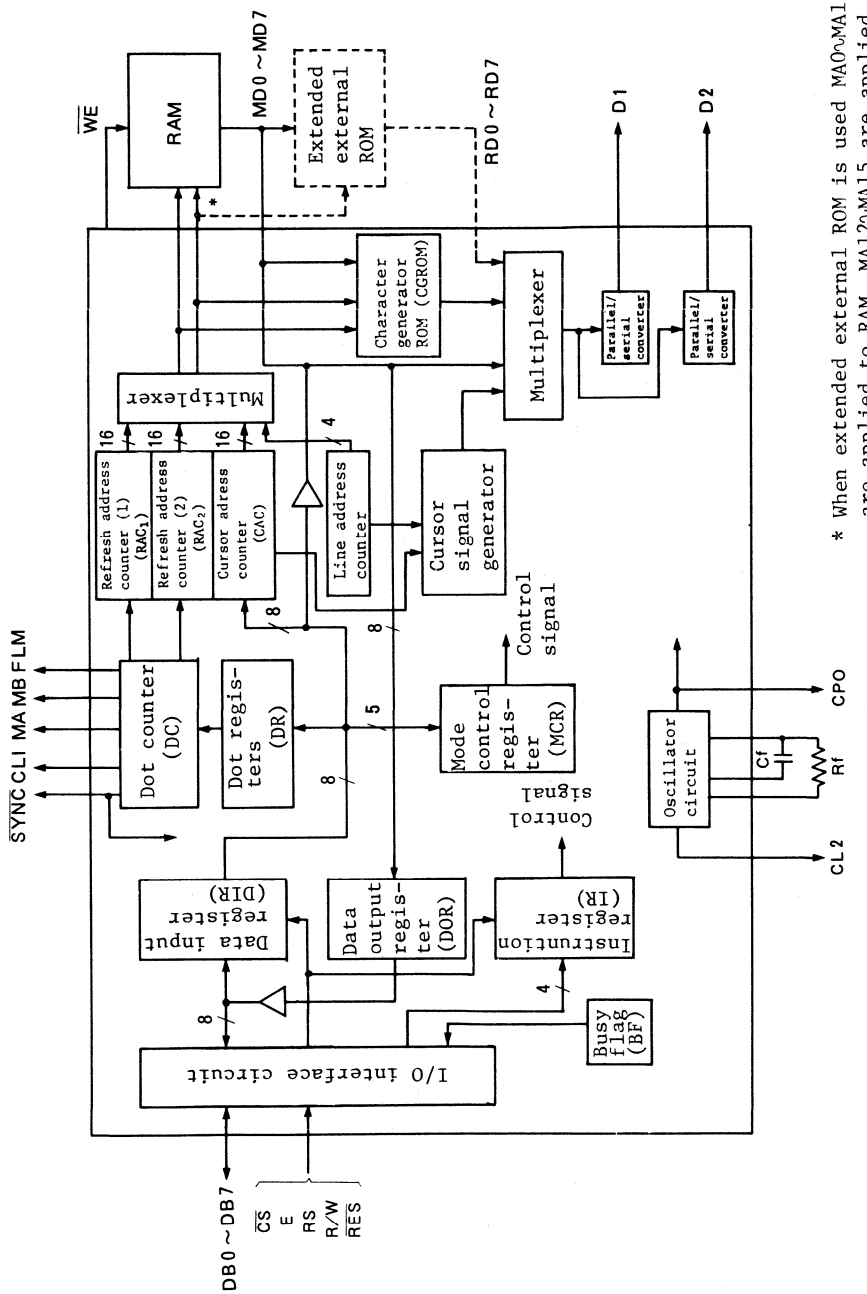


(Top View)

■ FEATURES

- Dot matrix liquid crystal graphic display controller
- Display control capacity
  Graphic mode ..... 512K dots (2^{16} bytes)
  Character mode ..... 4096 characters (2^{12} characters)
- Internal character generator ROM ..... 7360 bits
  160 types of 5×7 dot character fonts
  32 types of 5×11 dot character fonts
  Total 192 types
  (Can be extended to 256 types (4K bytes max.) by external ROM)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  Static to 1/128 duty selectable
- Various instruction functions
  Scroll, Cursor ON/OFF/blink, Character blink, Bit manipulation
- Display method ..... Selectable A or B types
- Internal oscillator (with external resistor and capacitor)
- Low power dissipation
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package

■BLOCK DIAGRAM



* When extended external ROM is used MA0∿MA11 are applied to RAM, MA12∿MA15 are applied to extended external ROM.

■BLOCK FUNCTIONS

●Registers

The HD61830 has the five types of registers: instruction register (IR), data input register (DIR), data output register (DOR), dot registers (DR) and mode control register (MCR).

The IR is a 4-bit register which stores the instruction codes for specifying MCR, DR, a start address register, a cursor address register and so on. The lower order 4 bits DB0 to DB3 of data buses are written in it.

The DIR is an 8-bit register used to temporarily store the data written into the external RAM, DR, MCR and so on.

The DOR is an 8-bit register used to temporarily store the data read from the external RAM. Cursor address information is written into the CAC through the DIR. When the memory read instruction is set in the IR (latched at the falling edge of E signal), the data of external RAM is read to DOR by an internal operation. The data is transferred to the MPU by reading the DOR with the next instruction (the contents of DOR are output to the data bus when E is at "High" level).

The DR are registers used to store the dot informations such as character pitches and the number of vertical dots and so on. The information sent from the MPU is written into the DR via the DIR.

The MCR is a 6-bit register used to store the data which specifies states of display such as display ON/OFF and cursor ON/OFF/blink. The information sent from the MPU is written in it via the DIR.

● Busy Flag (BF)

With "1", the busy flag indicates the HD61830 is performing an internal operation. The next instruction cannot be accepted. As shown in Control Instruction(14),the busy flag is output on DB7 under the conditions of RS=1, R/W=1 and E=1. Make sure the busy flag is "0" before writing the next instruction.

● Dot Counters (DC)

The dot counters are counters that generate liquid crystal display timing according to the contents of DR.

● Refresh Address Counters (RAC1/RAC2)

The refresh address counters are counters used to control the addresses of external RAM, having the two types: RAC1 and RAC2. The RAC1 is used for upper half of screen and the RAC2 for lower half. In the graphic mode, 16-bit data is output and used as the address signal of external RAM. In the character mode, the high order 4 bits (MA12∿MA15) are ignored. The 4 bits of line address counter are output and used as the address of extended ROM.

● Character Generator ROM

The character generator ROM has 7360 bits in total and stores 192 types of character data. A character code (8 bits) from the external RAM and a line code (4 bits) from the line address counter are applied to its address signals, and it outputs 5-bit dot data.

The character font is 5×7 (160 types) or 5×11 (32 types). The use of extended ROM allows 8×16 (256 types max.) to be used.

● Cursor Address Counter

The cursor address counter is a 16-bit counter that can be preset by the instruction. It is used to hold an address when the data of external RAM is read or written (when display dot data or a character code is read or written). The value of cursor address counter is automatically increased after the display data is read or written and after the Set/Clear Bit instruction is executed.

● Cursor Signal Generator

The cursor can be displayed by the instruction in the character mode. The cursor is automatically generated on the display specified by the cursor address and cursor position.

● Parallel/Serial Conversion

The parallel data sent from the external RAM, character generator ROM or extended ROM is converted into serial data by two parallel/serial conversion circuits and transferred to the liquid crystal driver circuits for upper screen and lower screen simultaneously.

■TERMINAL FUNCTIONS

Name	Function
DB0∿7	Data bus ... Three-state I/O common terminal Data is transferred to MPU through DB0 to DB7.
$\overline{CS}$	Chip select ... Selected state with $\overline{CS}$=0.
R/W	Read/Write ... R/W=1 ... MPU ← HD61830 R/W=0 ... MPU → HD61830
RS	Register select ... RS=1 ... Instruction register RS=0 ... Data register
E	Enable ... Data is written at the fall of E. Data can be read while E is 1.
CR, R, C	CR oscillator
$\overline{RES}$	Reset ... Reset=0 results in display OFF and slave mode.
MA0∿15	External RAM address output In character mode, the line code for external CG is output through MA12 to MA15 ("0": Character 1st line, "F": Character 16th line).
MD0∿7	Display data bus ... Three-state I/O common terminal.
RD0∿7	ROM data input ... Dot data from external character generator is input.
$\overline{WE}$	Write enable ... Write signal for external RAM.
CL2	Display data shift clock for LCD drivers.
CL1	Display data latch signal for LCD drivers.
FLM	Frame signal for display synchronization.
MA	Signal for converting liquid crystal driving signal into AC, A type
MB	Signal for converting liquid crystal driving signal into AC, B type
D1, D2	Display data serial output D1 ... For upper half of screen D2 ... For lower half of screen
CPO	Clock signal for HD61830 in slave mode.
$\overline{SYNC}$	Synchronous signal for parallel operation. Three-state I/O common terminal (with pull-up MOS). Master ... Synchronous signal is output. Slave ... Synchronous signal is input.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V	(1)
Terminal voltage	V_T	-0.3 ∿ V_{CC}+0.3	V	(1)
Operating temperature	T_{opr}	-20 ∿ +75	°C	
Storage temperature	T_{stg}	-55 ∿ +125	°C	

Note 1: All voltage is referenced to GND=0.

■ELECTRICAL CHARACTERISTICS

(V_{CC}=5V±5%, GND=0V, Ta=-20∿+75°C)

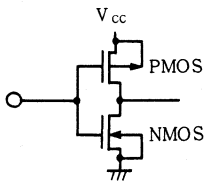
Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
Input "High" voltage (TTL)	V_{IH}		2.2	-	V_{CC}	V	(2)
Input "Low" voltage (TTL)	V_{IL}		0	-	0.8	V	(3)
Input "High" voltage	V_{IHR}		3.0	-	V_{CC}	V	(4)
Input "High" voltage (CMOS)	V_{IHC}		0.7V_{CC}	-	V_{CC}	V	(5)
Input "Low" voltage (CMOS)	V_{ILC}		0	-	0.3V_{CC}	V	(5)
Output "High" voltage (TTL)	V_{OH}	$-I_{OH}$=0.6mA	V_{CC}-0.4	-	V_{CC}	V	(6)
Output "Low" voltage (TTL)	V_{OL}	I_{OL}=1.6mA	0	-	0.4	V	(6)
Output "High" voltage(CMOS)	V_{OHC}	$-I_{OH}$=0.6mA	V_{CC}-0.4	-	V_{CC}	V	(7)
Output "Low" voltage (CMOS)	V_{OLC}	I_{OL}=0.6mA	0	-	0.4	V	(7)
Leakage current	I_{IN}	V_{IN}=0∿V_{CC}	-5	-	5	µA	(8)
Output leakage current	I_{OUT}	V_{OUT}=0∿V_{CC}	-10	-	10	µA	(9)
Power dissipation (1)	P_{w1}	CR oscillation fosc=500kHz	-	10	15	mW	(10)
Power dissipation (2)	P_{w2}	External clock fcp=1MHz	-	20	30	mW	(10)
Internal clock operation							
Clock oscillation frequency	f_{osc}	Cf=15pF±5% Rf=39kΩ±2%	350	500	650	kHz	(11)

Item	Symbol	Test condition	Min.	Typ	Max.	Unit	Note
External clock operation							
External clock operating frequency	f_{cp}		100	500	1100	kHz	(12)
External clock duty	Duty		47.5	50	52.5	%	(12)
External clock rise time	t_{rcp}		-	-	0.05	µs	(12)
External clock fall time	t_{fcp}		-	-	0.05	µs	(12)
Pull-up current	I_{PL}	V_{IN}=GND	2	10	20	µA	(13)

Note: The I/O terminals are of the following configuration:

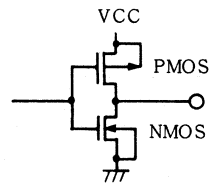
● Shape of Input Terminal

Applicable terminal: $\overline{CS}$, E, RS, R/W, $\overline{RES}$, RD0 to RD7, CR



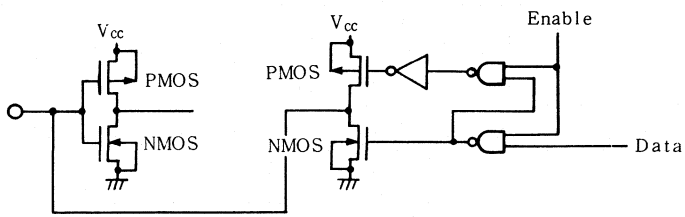
● Shape of Output Terminal

Applicable terminal: CL1, CL2, MA, MB, FLM, COP, D1, D2, $\overline{WE}$, MA0 MA15



● Shape of I/O Common Terminal

Applicable terminal: DB0∿DB7, $\overline{SYNC}$, MD0∿MD7



Note 2: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$, CR and $\overline{RES}$.

Note 3: Applied to input terminals and I/O common terminals, except terminals $\overline{SYNC}$ and CR.

Note 4: Applied to terminal $\overline{RES}$.

Note 5: Applied to terminals $\overline{SYNC}$ and CR.

Note 6: Applied to terminals DB0∿DB7, $\overline{WE}$, MA0∿MA15,and MD0∿MD7.

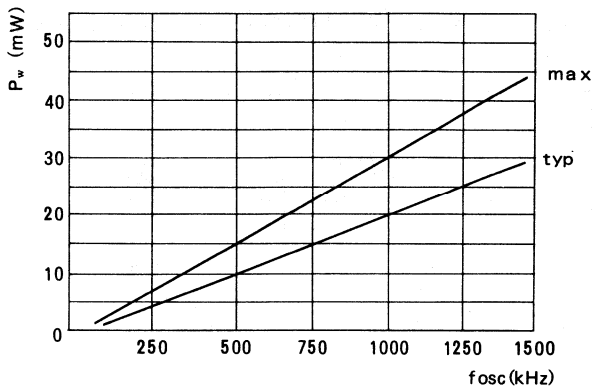
Note 7: Applied to terminals $\overline{SYNC}$, CP0, FLM, CL1, CL2, D1, D2, MA and MB.

Note 8: Applied to input terminals.

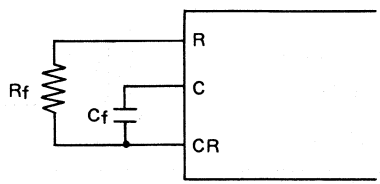
Note 9: Applied to I/O common terminals. However, the current which flows into the output drive MOS is excluded.

Note 10: The current which flows into the input and output circuits is excluded. When the input of CMOS is in the intermediate level, current flows through the input circuit, resulting in the increase of power supply current. To avoid this, input must be fixed at high or low.

The relationship between the operating frequency and the power dissipation is given below.

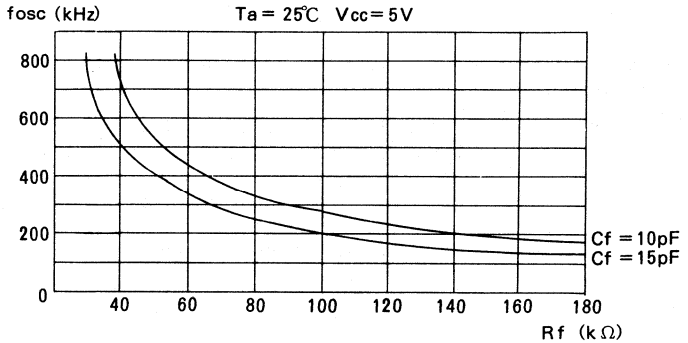


Note 11: Applied to the operation of internal oscillator when oscillation resistor Rf and oscillation capacity Cf are used.

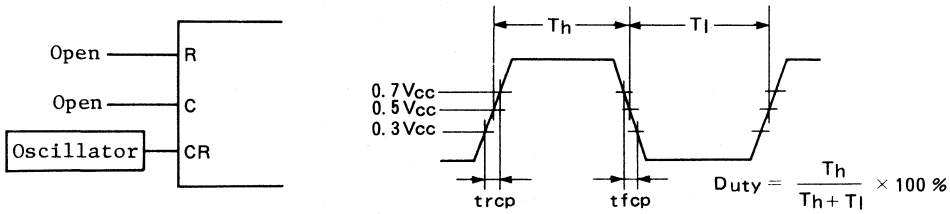


$C_f = 15pF \pm 5\%$
$R_f = 39k\Omega \pm 2\%$
(when fosc = 500kHz typ)

The relationship among oscillation frequency, Rf and Cf is given below.



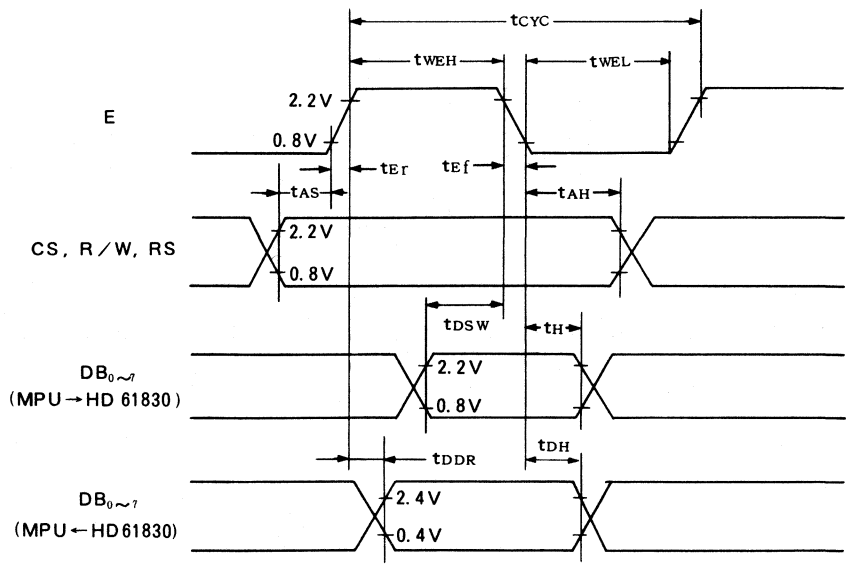
Note 12: Applied to external clock operation.



Note 13: Applied to $\overline{SYNC}$, DB0∿DB7, and RD0∿RD7.

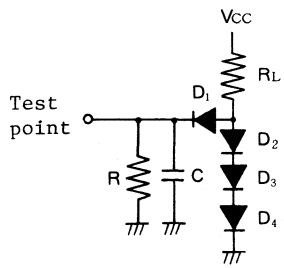
■TIMING CHARACTERISTICS

●Bus Read/Write Operation (Interface to MPU)



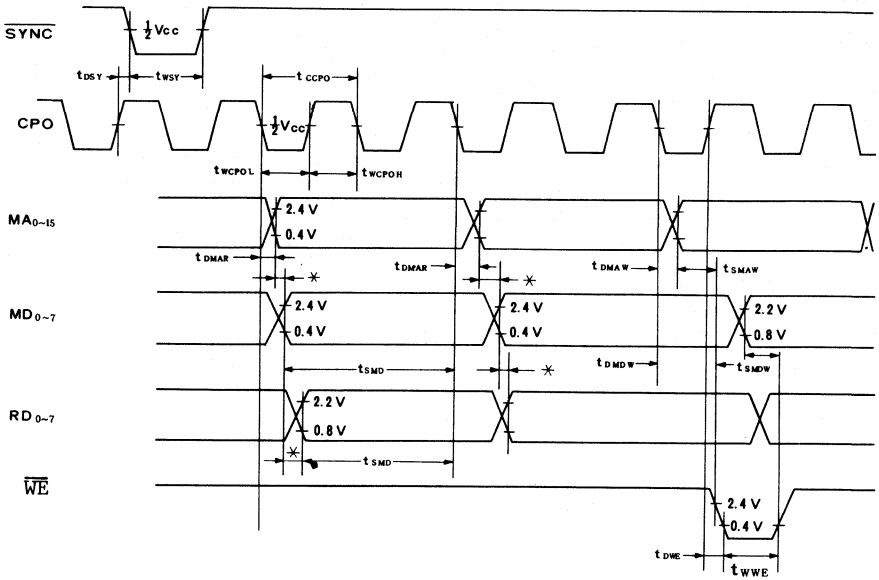
Item		Symbol	Min.	Typ	Max.	Unit	
Enable cycle time		t_{CYC}	1.0	-	-	µs	
Enable pulse width	"High" level	t_{WEH}	0.45	-	-	µs	
	"Low" level	t_{WEL}	0.45	-	-	µs	
Enable rise time		t_{Er}	-	-	25	ns	
Enable fall time		t_{Ef}	-	-	25	ns	
Setup time		t_{AS}	140	-	-	ns	
Data setup time		t_{DSW}	225	-	-	ns	
Data delay time		t_{DDR}	-	-	225	ns	Note
Data hold time		t_H	10	-	-	ns	
Address hold time		t_{AH}	10	-	-	ns	
Data hold time		t_{DH}	20	-	-	ns	

Note: The following load circuit is connected for specification:



R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF
Diodes D1 to D4: 1S2074 Ⓗ

●Interface to External RAM and ROM

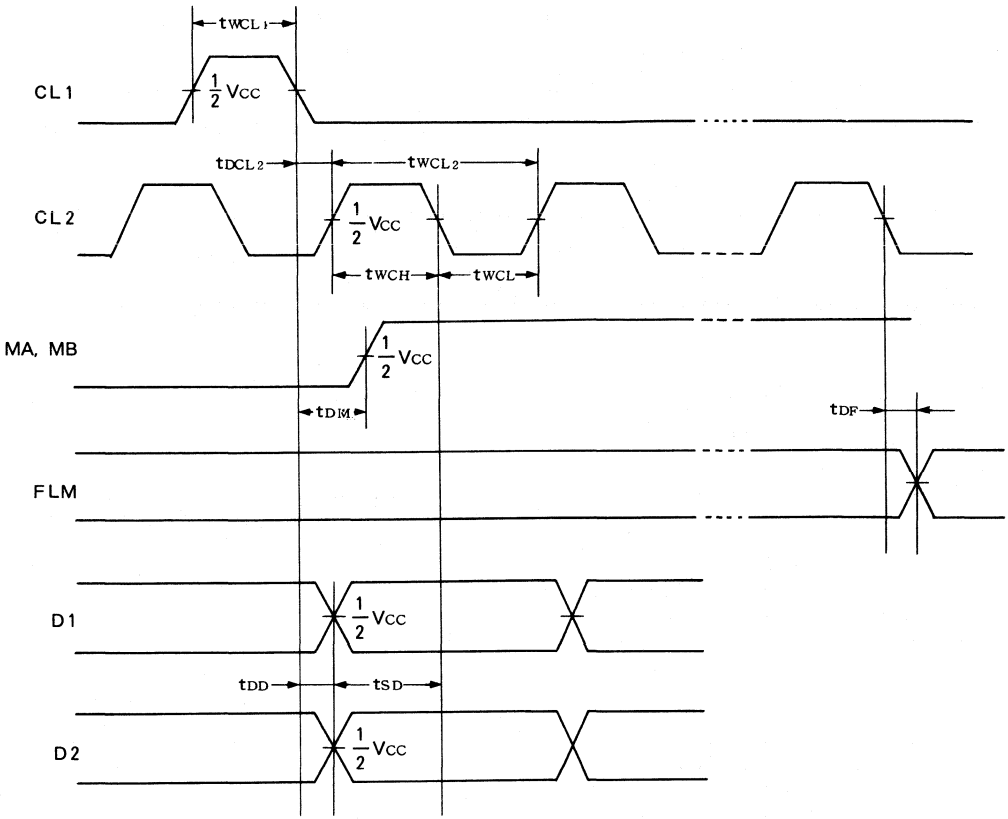


Item		Symbol	Min.	Typ	Max.	Unit
$\overline{SYNC}$ delay time		t_{DSY}	-	-	200	ns
$\overline{SYNC}$ pulse width	"High" level	t_{WSY}	900	-	-	ns
CPO cycle time		t_{CCPO}	900	-	-	ns
CPO pulse width	"High" level	t_{WCPOH}	450	-	-	ns
	"Low" level	t_{WCPOL}	450	-	-	ns
MA0 to MA15 refresh delay time		t_{DMAR}	-	-	200	ns
MA0 to MA15 write address delay time		t_{DMAW}	-	-	200	ns
MD0 to MD7 write data delay time		t_{DMDW}	-	-	200	ns
MD0 to MD7, RD0 to RD7 setup time		t_{SMD}	900	-	-	ns
Memory address setup time		t_{SMAW}	250	-	-	ns
Memory data setup time		t_{SMDW}	250	-	-	ns
$\overline{WE}$ delay time		t_{DWE}	-	-	200	ns
$\overline{WE}$ pulse width ("Low" level)		t_{WWE}	450	-	-	ns

Note 1: No load is applied to all the output terminals.

Note 2: "*" indicates the delay time of RAM and ROM.

● Data Transfer to Driver LSI



Item		Symbol	Min.	Typ	Max.	Unit
Clock pulse width ("High" level)		t_{WCL1}	450	-	-	ns
Clock delay time		t_{DCL2}	-	-	200	ns
Clock cycle time		t_{WCLZ}	900	-	-	ns
Clock pulse width	"High" level	t_{WCH}	450	-	-	ns
	"Low" level	t_{WCL}	450	-	-	ns
Data delay time		t_{DM}	-	-	300	ns
Data delay time		t_{DF}	-	-	300	ns
Data delay time		t_{DD}	-	-	200	ns
Data setup time		t_{SD}	250	-	-	ns

Note: No load is applied to all the output terminals (MA, MB, FLM, D1 and D2).

● Display Control Instructions

Display is controlled by writing data into the instruction register and 13 data registers. The RS signal distinguishes the instruction register from the data registers. 8-bit data is written into the instruction register with RS=1, and the code of data register is specified. The 8-bit data is written in the data register and the specified instruction is executed with RS=0.

During the execution of the instruction, no new instruction can be accepted. Since the busy flag is set during this, read the busy flag and make sure it is 0 before writing the next instruction.

(1) Mode control

Code $"00" (hexadecimal) written into the instruction register specifies the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	0
Mode control reg.	0	0	0	0	Mode data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	0	0	0	0	Cursor OFF	Internal CG	Character display (Character mode)
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF, character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
Display ON/OFF	Master/ slave	Blink	Cursor	Graphic/ character mode	Ext./ Int.CG			

1: Master mode
0: Slave mode

1: Display ON
0: Display OFF

(2) Set character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	0	1
Character pitch reg.	0	0	(V_p - 1) binary				0	(H_p - 1) binary		

Vp indicates the number of vertical dots per character. The space between the vertically-displayed characters is considered for determination. This value is meaningful only during character display (in the character mode) and becomes invalid in the graphic mode.

The Hp indicates the number of horizontal dots per character in display, including the space between horizontally-displayed characters. In the graphic mode, the Hp indicates the number of bits of 1-byte display data to be displayed.

There are three Hp values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	" 7
8	1	1	1	" 8

(3) Set number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	0
Number-of-characters reg.	0	0	0	(Hn - 1) binary						

Hn indicates the number of horizontal characters in the character mode or the number of horizontal bytes in the graphic mode. If the sum total of horizontal dots on the screen is taken as n,

$$n = Hp \times Hn$$

Hn can be set with an even number of 2 to 128 (decimal).

(4) Set number of time division (inverse of display duty ratio)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	0	1	1
Number-of-time shares reg.	0	0	0	(Nx - 1) binary						

Nx indicates the number of time division in multiplex display.
1/Nx is a display duty ratio.

A value of 1 to 128 (decimal) can be set to Nx.

(5) Set cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	0	1	0	0
Cursor position reg.	0	0	0	0	0	0	(Cp - 1) binary			

Cp indicates the position in a character where the cursor is displayed in the character mode. For example, in 5×7 dot font, the cursor is displayed under a character by specifying Cp=8 (decimal). The cursor horizontal length is equal to the horizontal character pitch Hp. A value of 1 to 16 (decimal) can be set to Cp. If a smaller value than the number of vertical character pitches Vp is set ($Cp \leqq Vp$), and a character is overlapped with the cursor, the cursor has higher priority of display (at cursor display ON). If Cp is greater than Vp, no cursor is displayed. The cursor horizontal length is equal to Hp.

(6) Set display start low order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	0
Display start address reg. (low order byte)	0	0	(Start low order address) binary							

(7) Set display start high order address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	0	1
Display start address reg. (high order byte)	0	0	(Start high order address) binary							

These instructions cause display start addresses to be written in the display start address registers. The display start address indicates a RAM address at which the data displayed at the top left end on the screen is stored. In the graphic mode, the start address is composed of high/low order 16 bits. In the character display, it is composed of the lower 4 bits of high order address and 8 bits of low order address. The upper 4 bits of high order address are ignored.

(8) Set cursor address (low order) (RAM write low order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	0
Cursor address counter (low order byte)	0	0	(Cursor low order address) binary							

(9) Set cursor address (high order) (RAM write high order address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	0	1	1
Cursor address counter (high order byte)	0	0	(Cursor high order address) binary							

These instructions cause cursor addresses to be written in the cursor address counters. The cursor address indicates an address for sending or receiving display data and character codes to or from the RAM. In the character mode, the cursor is displayed at the digit specified by the cursor address.

(10) Write display data

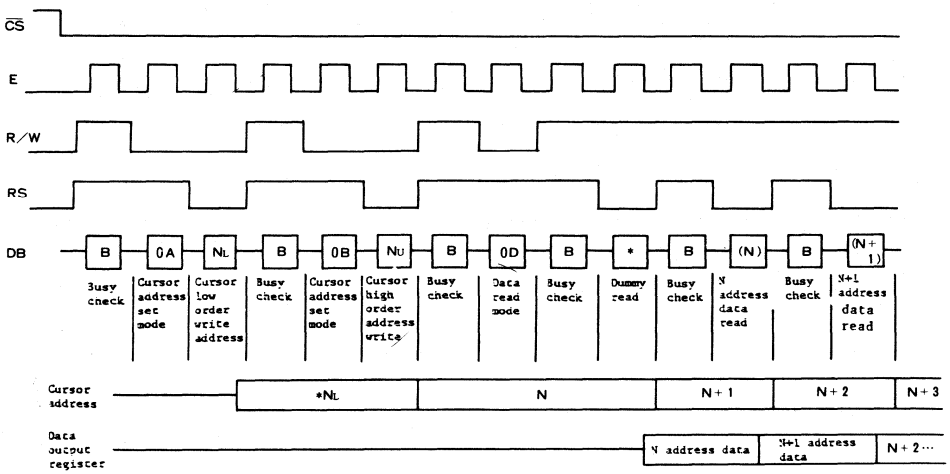
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code) LSB							

After the code $'0C' is written into the instruction register with RS=1, 8 bit data with RS=0 should be written into the data register. This data is transferred to the RAM specified by the cursor address. The cursor address is increased by 1 after this operation.

(11) Read display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code) LSB							

Data can be read from the RAM by writing code $'0D' into the instruction register with RS=0. The read procedure is as follows:



This instruction outputs the contents of data output register on Data Bus (DB0 to DB7) and then transfers RAM data specified by a cursor address to the data output register, also increasing the cursor address by 1. After setting the cursor address, correct data is not output at the first read but at the second time. Thus, make one dummy read when reading data after setting the cursor address.

(12) Clear bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	0
Bit clear reg.	0	0	0	0	0	0	0	(N_B - 1) binary		

(13) Set bit

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction reg.	0	1	0	0	0	0	1	1	1	1
Bit set reg.	0	0	0	0	0	0	0	(N_B - 1) binary		

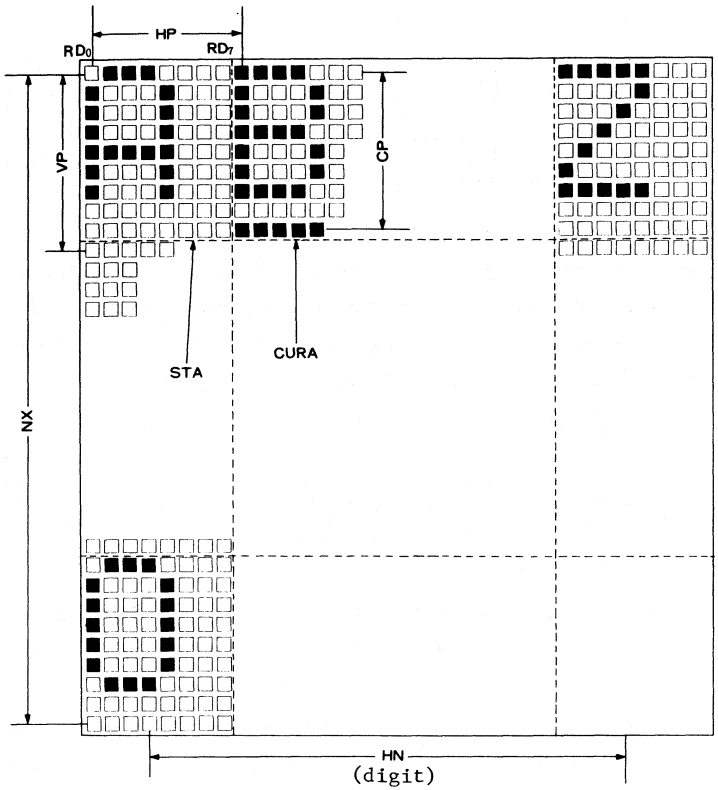
The Clear/Set Bit instruction sets 1 bit in a byte of display data RAM to 0 or 1, respectively. The position of the bit in a byte is specified by N_B. After the execution of the instruction, the cursor address is automatically increased by 1. N_B is a value of 1 to 8. N_B=1 and N_B 8 indicates LSB and MSB, respectively.

(14) Read busy flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	1/0							

When the read mode is set with RS=1, the busy flag is output to DB7. The busy flag is set to 1 during the execution of any of instructions (1) to (13). After the execution, it is set to 0. The next instruction can be accepted. No instruction can be accepted when busy flag=1. Before executing an instruction or writing data, perform a busy flag check to make sure the busy flag is 0. When data is written in the register (RS=1), no busy flag changes. Thus, no busy flag check is required just after the write operation into the instruction register with RS=1.

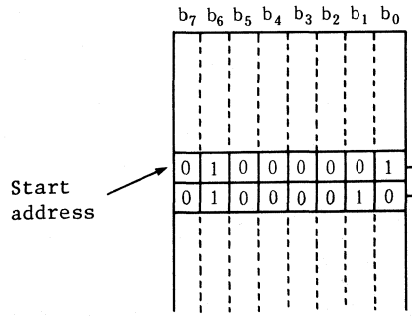
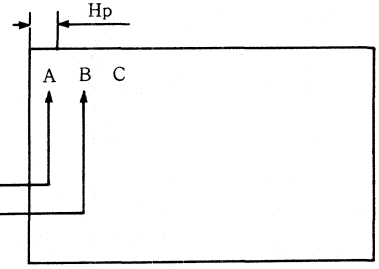
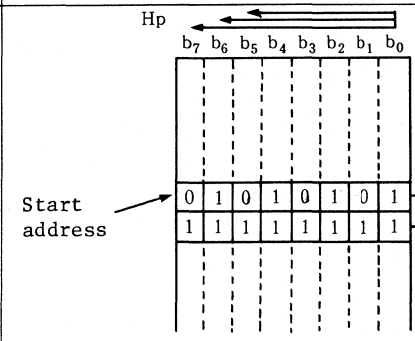
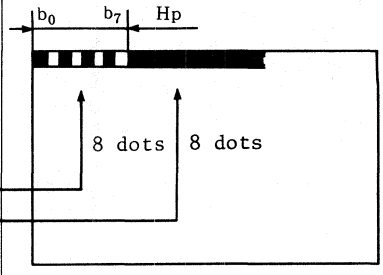
The busy flag can be read without specifying any instruction register.



Symbol	Name	Meaning	Value
H_p	Horizontal character pitch	Lateral character pitch	6 to 8 dots
H_N	Number of horizontal characters	Number of lateral characters per line (number of digits) in the character mode or number of bytes per line in the graphic mode.	2 to 128 digits (an even number)
V_p	Vertical character pitch	Longitudinal character pitch	1 to 16 dots
C_p	Cursor position	Line number on which the cursor can be displayed	1 to 16 line
N_x	Number of time division	Inverse of display duty ratio	1 to 128 lines

Note: If the number of vertical dots on screen is taken as m, and the number of horizontal dots as n,

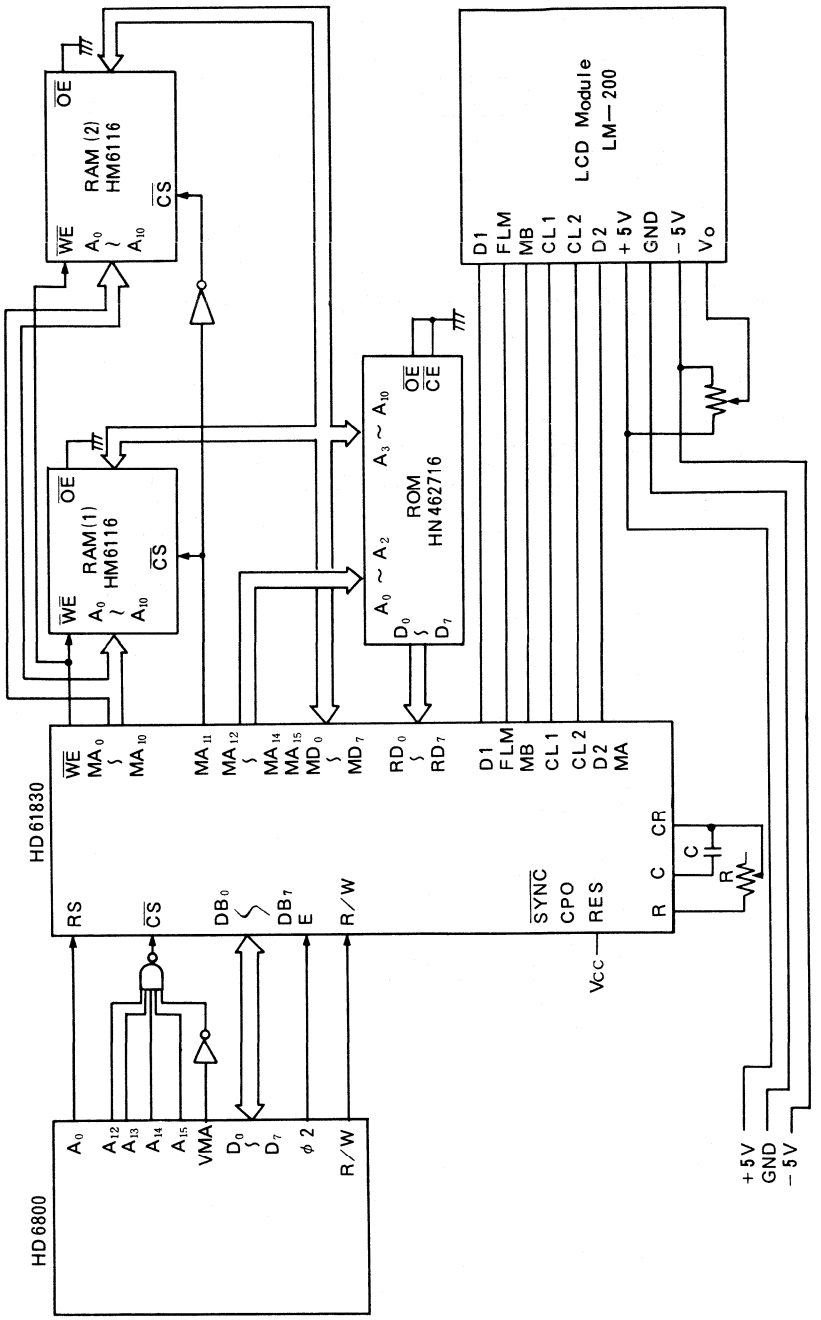
$1/m = 1/Nx$ = display duty ratio
$n = Hp \times Hn$, m/Vp = No. of display lines
$Cp \leqq Vp$

Display mode	Display data from MPU	RAM	Liquid crystal display panel
Character dispaly	Character code (8 bits)		
Graphic	Display pattern (8 bits)		

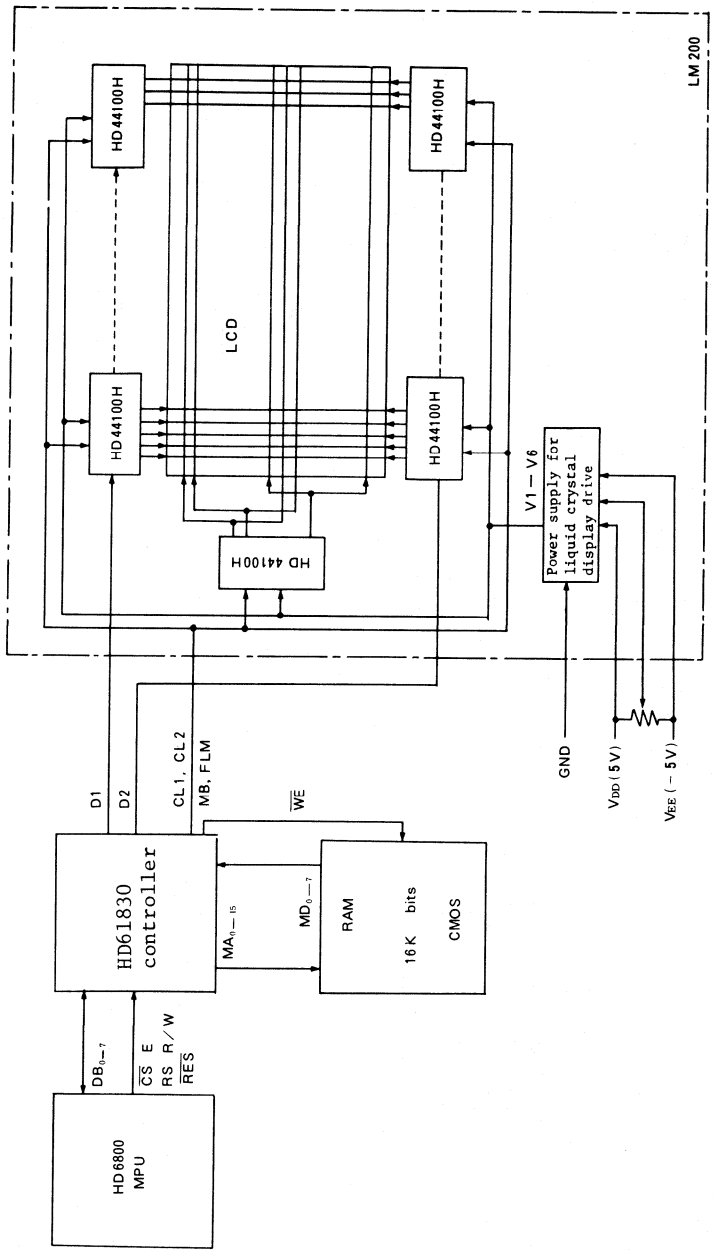
● Internal Character Generator Patterns and Character Codes

Higher / Lower 4bit / 4bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000												
××××0001												
××××0010												
××××0011												
××××0100												
××××0101												
××××0110												
××××0111												
××××1000												
××××1001												
××××1010												
××××1011												
××××1100												
××××1101												
××××1110												
××××1111												

■APPLICATION (CHARACTER MODE, EXTERNAL CG, CHARACTER FONT 8×8)

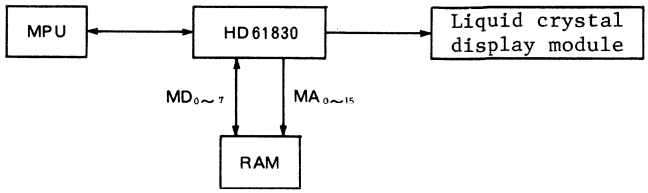


■APPLICATION (GRAPHIC MODE)

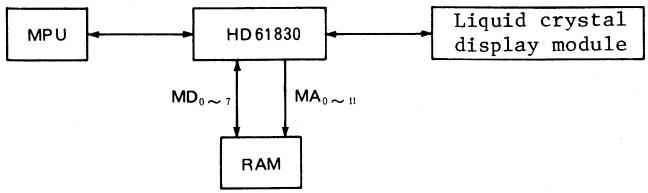


■EXAMPLE OF CONFIGURATION

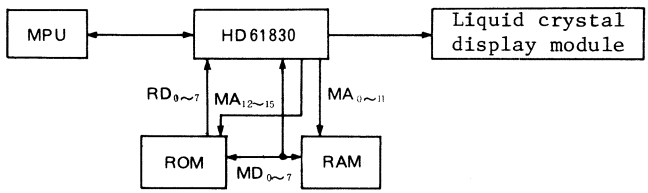
●Graphic Mode



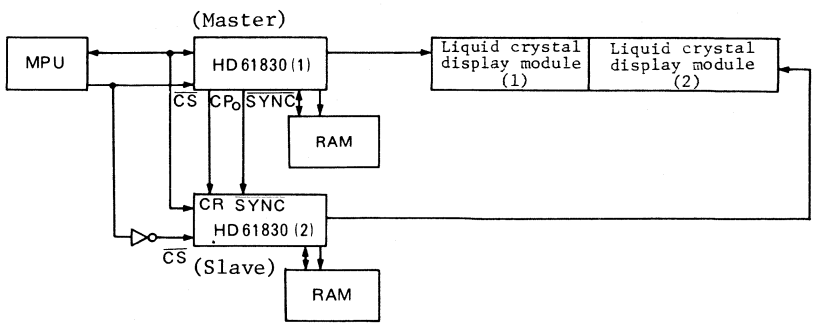
●Character Mode (1) (Internal Character Generator)



●Character Mode (2) (External Character Generator)



●Parallel Operation

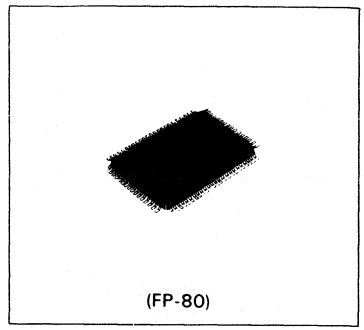


HD61602/HD61603
(SEGMENT TYPE LCD DRIVER)

The HD61602 and the HD61603 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microcomputers such as the HMCS6800 series.

The HD61602 incorporates the power supply circuit for liquid crystal display driver. By the software-controlled liquid crystal driving method, several types of liquid crystals can be connected according to the applications.

The HD61603 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.



■ FEATURES

- Wide-range operating voltage

  Operates in a wide range of supply voltage 2.2V to 5.5V.
  Compatible with TTL interface at 4.5V to 5.5V.

- Low current consumption

  Can drive from a battery power supply (100μA max. on 5V).
  Standby input enables a standby operation at lower current consumption (5μA max. on 5V).

- Internal power supply circuit for liquid crystal display driver (HD61602).

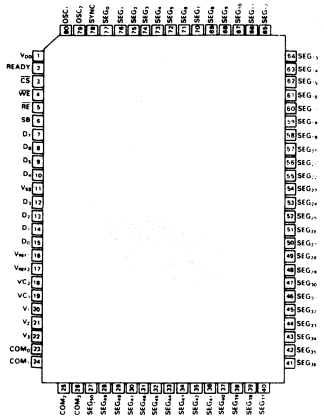
  Internal power supply circuit for liquid crystal display driver facilitates the connection to a microcomputer system.

- Versatile segment driving capacity

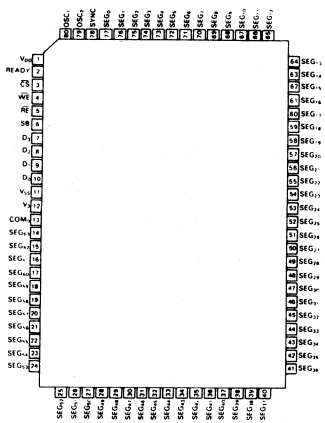
Type No.	Driving method		Display segments	Example of use
HD61602	Static		51	8 segments × 6 digits + 3 marks
	1/2 bias	1/2 duty	102	8 segments × 12 digits + 6 marks
	1/3 bias	1/3 duty	153	9 segments × 17 digits
		1/4 duty	204	8 segments × 25 digits + 4 marks
HD61603	Static		64	8 segments × 8 digits

■ PIN ARRANGEMENT (TOP VIEW)

HD61602

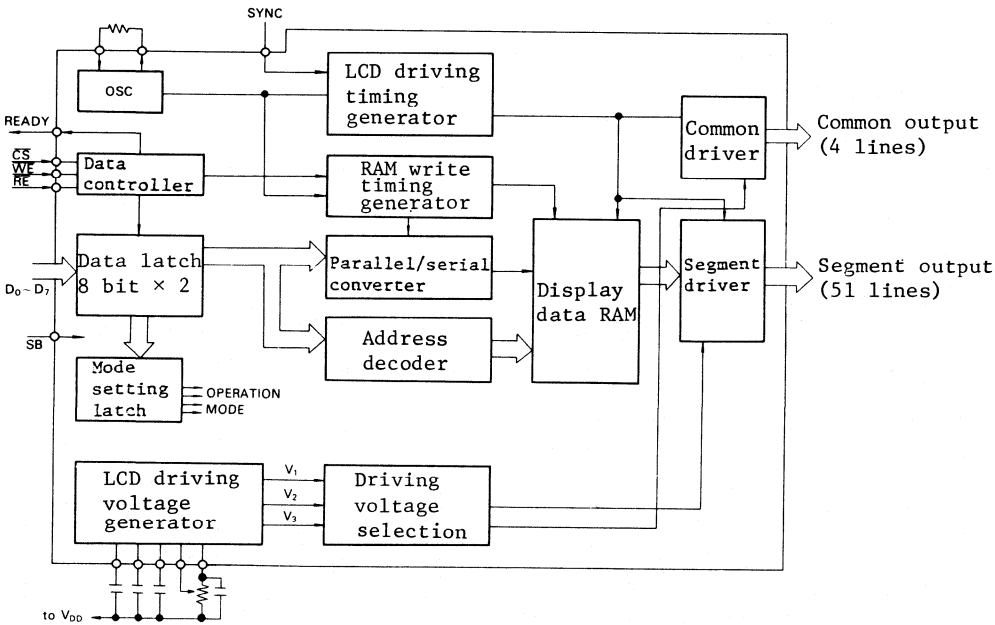


HD61603

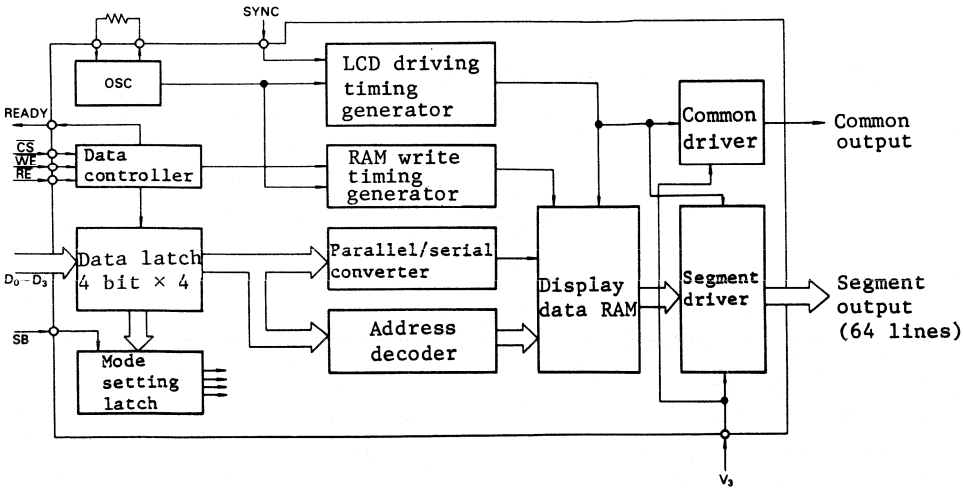


■ BLOCK DIAGRAM

● HD61602



● HD61603



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Limit	Unit
Power supply voltage*	V_{SS}, V1, V2, V3	0.3 ∿ -7.0	V
Terminal voltage*	V_T	0.3 ∿ V_{SS}-0.3	V
Operating temperature	T_{opr}	-20 ∿ +75	°C
Storage temperature	T_{stg}	-55 ∿ +125	°C

* Value referred to V_{DD}=0V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Limit			Unit
		Min.	Typ	Max.	
Power supply voltage*	$-V_{SS}$	2.2	-	5.5	V
	-V1, -V2, -V3	0	-	5.5	V
Terminal voltage*	$-V_T$	0	-	$-V_{SS}$	V
Operating temperature	T_{opr}	-20	-	75	°C

* Value referred to V_{DD}=0V.

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics (1)

(V_{SS}=0V, V_{DD}=4.5 to 5.5V, Ta=-20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Input "High" voltage	OSC1	V_{IH1}		0.8V_{DD}	-	V_{DD}	V
	Others	V_{IH2}		2.0	-	V_{DD}	V
Input "Low" voltage	OSC1	V_{IL1}		0	-	0.2V_{DD}	V
	Others	V_{IL2}		0	-	0.8	V
Output leakage current	READY	I_{OH}	V_O=V_{DD}	-	-	5	μA
Output "Low" voltage	READY	V_{OL}	I_{OL}=0.4mA	-	-	0.4	V
Input leakage current		I_{IL}	V_{IN}=0∿V_{DD}	-1.0	-	1.0	μA
LCD driver voltage drop	COM0∿COM3	V_{d1}	±Id=3μA for each COM	-	-	0.3	V
	SEG0∿SEG50	V_{d2}	±Id=3μA for each SEG	-	-	0.6	V
Power supply current		I_{DD}	During display*	-	-	100	μA
		I_{DD}	At standby	-	-	5	μA

* Except the transfer operation of display data and bit data.

● DC Characteristics (2)

(V_{SS}=0V, V_{DD}=2.2 to 3.8V, Ta=-20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Input "High" voltage		V_{IH}		0.8V_{DD}	-	V_{DD}	V
Input "Low" voltage		V_{IL}		0	-	0.2V_{DD}	V
Output leakage current	READY	I_{OH}	V_{IN}=V_{DD}	-	-	5	μA
Output "Low" voltage	READY	V_{OL}	I_{OL}=0.04mA	-	-	0.1V_{DD}	V
Input leakage current		I_{IL}	V_{IN}=0∿V_{SS}	-1.0	-	1.0	μA
LCD driver voltage drop	COM0∿COM3	V_{d1}	±Id=3μA for each COM	-	-	0.3	V
	SEG0∿SEG50	V_{d2}	±Id=3μA for each SEG	-	-	0.6	V
Power supply current		I_{SS}	During display*	-	-	50	μA
		I_{SS}	At standby	-	-	5	μA

* Except the transfer operation of display data and bit data.

● AC Characteristics (1)

(V_{SS}=0V, V_{DD}=4.5 to 5.5V, Ta=-20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Oscillation frequency	OSC2	f_{osc}	R_{osc}=360kΩ	-	100	-	kHz
External clock frequency	OSC1	f_{osc}		-	100	-	kHz
External clock duty	OSC1	Duty		40	50	60	%
I/O signal timing		t_S		400	-	-	ns
		t_H		10	-	-	ns
		t_{WH}		300	-	-	ns
		t_{WL}		400	-	-	ns
		t_{WR}		400	-	-	ns
		t_{DL}	Fig. 5	-	-	600	ns
		t_{EN}		400	-	-	ns
		t_{OP1}	For display data transfer	10.5	-	11.5	Clock
		t_{OP2}	For bit and mode data transfer	3.5	-	4.5	Clock
Input signal rise time and fall time		t_r, t_f		-	-	25	ns

● AC Characteristics (2)

(V_{SS}=0V, V_{DD}=2.2 to 3.8V, Ta=-20 to +75°C, unless otherwise noted)

Item		Symbol	Test condition	Limit			Unit
				Min.	Typ	Max.	
Oscillation frequency	OSC2	f_{osc}	R_{osc}=330kΩ	-	100	-	kHz
External clock frequency	OSC1	f_{osc}		-	100	-	kHz
External clock duty	OSC1	Duty		40	50	60	%
I/O signal timing		t_S		1.5	-	-	µs
		t_H		1.0	-	-	µs
		t_{WH}		1.5	-	-	µs
		t_{WL}		1.5	-	-	µs
		t_{DL}	Fig. 6	-	-	2.0	µs
		t_{WR}		1.5	-	-	µs
		t_{EN}		2.0	-	-	µs
		t_{OP1}	For display data transfer	10.5	-	11.5	Clock
		t_{OP2}	For bit and mode data transfer	3.5	-	4.5	Clock
Input signal rise time and fall time		t_r, t_f		-	-	5.0	µs

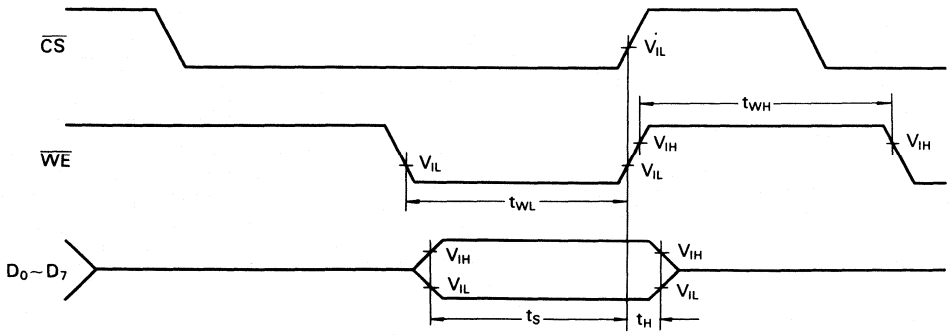


Fig. 1 Write Timing
($\overline{RE}$ is fixed on "High" level, and SYNC on "Low" level)

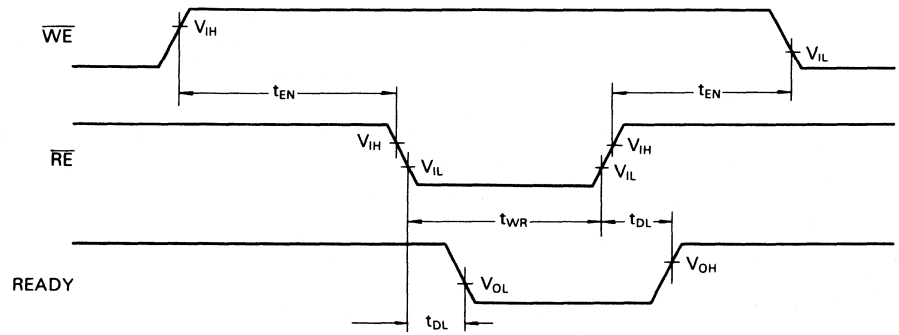


Fig. 2 Reset/Read Timing
($\overline{CS}$ and SYNC are fixed on "Low" level)

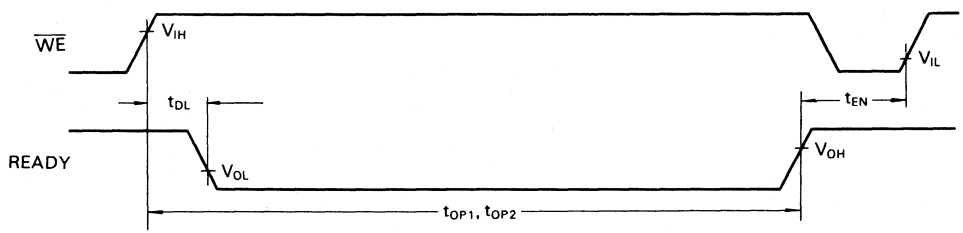


Fig. 3 READY Timing
(When the READY output is always available)

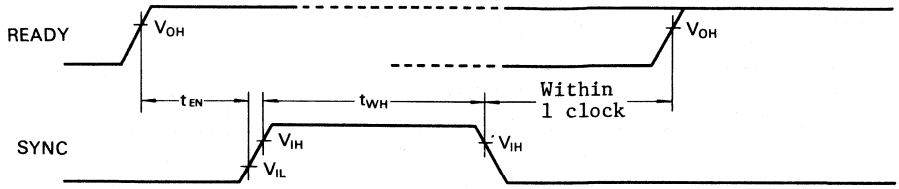


Fig. 4 SYNC Timing

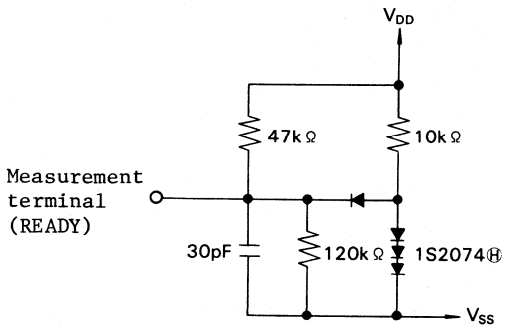


Fig. 5 Bus Timing Load Circuit
(LS-TTL Load)

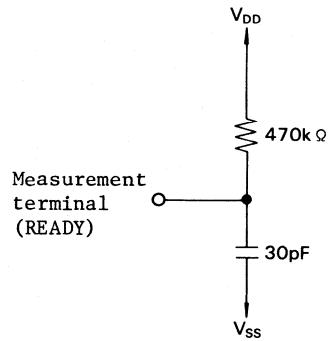


Fig. 6 Bus Timing Load Circuit
(CMOS Load)

■ TERMINAL FUNCTIONS

●HD61602 Terminal Functions

Terminal name	No. of lines	Input/output	Connected to	Function
V_{DD}	1	Power supply		⊕ -side power supply
READY	1	NMOS open drain output	MCU	During setting data in the display data RAM and mode setting latch in the LSI after data transfer, "Low" is output to the READY terminal to inhibit the next data input. There are two types of modes: one in which "Low" is output only when both of $\overline{CS}$ and $\overline{RE}$ are "Low", and the other in which "Low" is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is "Low".
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D7 is latched at the rising edge of $\overline{WE}$.
$\overline{RE}$	1	Input	MCU	Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are "Low", the first data is recognized as the 1st byte data.
SB	1	Input	MCU	"High" level input stops the LSI operations. (i) Stops oscillation and clock input. (ii) Stops LCD driver. (iii) Stops writing data into display RAM.
D0∿D7	8	Input	MCU	Data input terminal from where 8-bit × 2-byte data are input.
V_{SS}	1	Power supply		⊖ -side power supply
V_{REF1}	1	Output	External R	Reference voltage output. LCD driving voltage is generated by this voltage.
V_{REF2}	1	Input	External R	Divides the reference voltage of V_{REF1} with external R to determine LCD driving voltage. $V_{REF2} \fallingdotseq V1$

Terminal name	No. of lines	Input/output	Connected to	Function
V_{C1}, V_{C2}	2	Output	External C	Connection terminals for boosting C of LCD driving voltage generator. An external C is connected between V_{C1} and V_{C2}.
V1, V2, V3	3	Output (Input)	External C	LCD driving voltages are output. An external C is connected to each terminal.
COM0∿COM3	4	Output (Input)	LCD	LCD common (backplate) driving output.
SEG0∿SEG50	51	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips application. LCD driver timing circuit is reset by "High" input. LCD is off.
OSC1 OSC2	2	Input Output	External R	Attaches external R to these terminals for oscillation. An external clock (100kHz) can be input from OSC1.

Note: Logic polarity is positive. "1"="H"=active.

●HD61603 Terminal Functions

Terminal name	No. of lines	Input/output	Connected to	Function
V_{DD}	1	Power supply		⊕-side power supply
READY	1	NMOS open drain output	MCU	During setting data in the display data RAM and mode setting latch in the LSI after data transfer, "Low" is output to the READY terminal to inhibit the next data input. There are two types of modes: one in which "Low" is output only when both of $\overline{CS}$ and $\overline{RE}$ are "Low", and the other in which "Low" is output regardless of $\overline{CS}$ and $\overline{RE}$.
$\overline{CS}$	1	Input	MCU	Chip select input. Data can be written only when this terminal is "Low".
$\overline{WE}$	1	Input	MCU	Write enable input. Input data of D0 to D3 is latched at the rising edge of $\overline{WE}$.

Terminal name	No. of lines	Input/output	Connected to	Function
$\overline{RE}$	1	Input	MCU	Reset the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are "Low", the first data is recognized as the 1st byte data.
SB	1	Input	MCU	"High" level input stops the LSI operations. (i) Stops oscillation and clock input. (ii) Stops LCD driver. (iii) Stops writing data into display RAM.
D0∿D3	4	Input	MCU	Data input terminal from where 4-bit x4 data are input.
V_{SS}	1	Power supply		⊖-side power supply
V3	1	Input	Power supply	Power supply input for LCD drive. Voltage between V_{DD} and V3 is used as driving voltage.
COM0	1	Output	LCD	LCD common (backplate) driving output.
SEG0∿SEG63	64	Output	LCD	LCD segment driving output.
SYNC	1	Input	MCU	Synchronous input for 2 or more chips application. LCD driver timing circuit is reset by "High" input. LCD is off.
OSC1 OSC2	2	Input Output	External R	Attaches external R to these terminals for oscillation. An external clock (100kHz) can be input from OSC1.

Note: Logic polarity is positive. "1"="H"=active.

■ DISPLAY RAM

< HD61602 Display RAM >

The HD61602 has an internal display RAM shown in Fig. 7. Display data is stored in the RAM, or is read according to the LCD driving timing to display on the LCD. One bit of the RAM corresponds to the 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD driving mode.

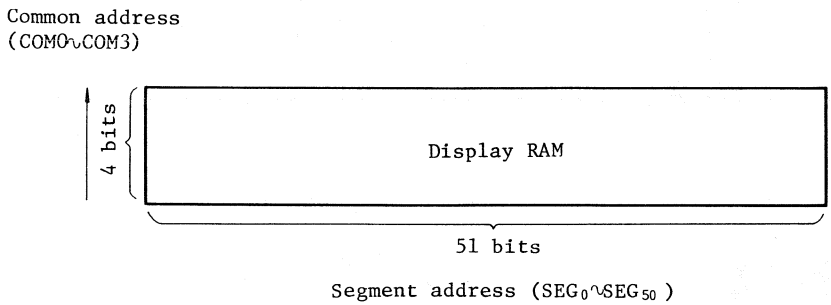


Fig. 7 Display RAM

● Reading Data from Display RAM

A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn terminal.

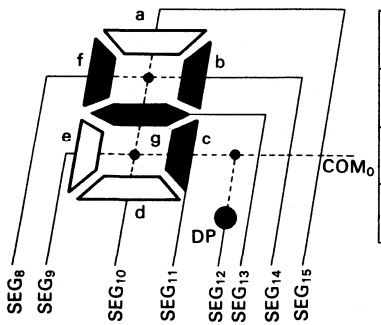
A common address corresponds to the output timings of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

When a 7-segment type LCD driver is connected, for example, the correspondence between the display RAM and the display pattern in each mode is as follows:

(1) Static drive

In the static drive, only the column of COM0 of display RAM is output. COM1 to COM3 are not displayed.

LCD connection

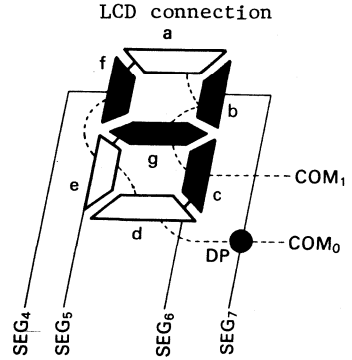


Display RAM

COM_3									
COM_2									
COM_1									
COM_0	f	e	d	c	DP	g	b	a	
	SEG_8	SEG_9	SEG_{10}	SEG_{11}	SEG_{12}	SEG_{13}	SEG_{14}	SEG_{15}	

(2) 1/2 duty drive

LCD connection



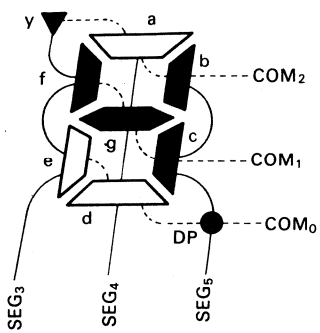
Display RAM

COM_3							
COM_2							
COM_1	a	g	c	b			
COM_0	f	e	d	DP			
	SEG_4	SEG_5	SEG_6	SEG_7	SEG_8	SEG_9	

In the 1/2 duty drive, the columns of COM0 and COM1 of display RAM are output in time sharing. The columns of COM2 and COM3 are not displayed.

(3) 1/3 duty drive

LCD connection



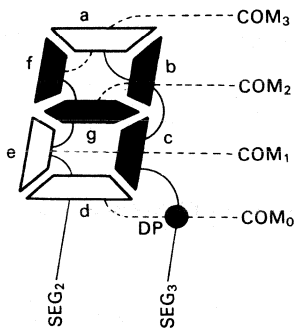
Display RAM

COM_3					
COM_2	y	a	b		
COM_1	f	g	c		
COM_0	e	d	DP		
	SEG_3	SEG_4	SEG_5	SEG_6	

In the 1/3 duty drive, the columns of COM0 to COM2 are output in time sharing. No column of COM3 is displayed.

(4) 1/4 duty drive

LCD connection



Display RAM

COM_3	f	a		
COM_2	g	b		
COM_1	e	c		
COM_0	d	DP		
	SEG_2	SEG_3	SEG_4	

In the 1/4 duty drive, all the columns of COM0 to COM3 are displayed.

●Writing Data into Display RAM

Data is written into the display RAM in the following five methods:

(1) Bit manipulation
Data is written into any bit of RAM on a bit basis.

(2) Static display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

(3) 1/2 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty drive.

(4) 1/3 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty drive.

(5) 1/4 duty display mode
8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the driving methods as described in the selection of "Reading Data from Display RAM".

8-bit data is written on a digit basis corresponding to the above duty driving methods. The digits are allocated as shown Fig. 8 (allocation of digit). As the data can be transferred on a digit basis from a microcomputer, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Fig. 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Fig. 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis, 8-bit display data and digit address should be specified as described above.

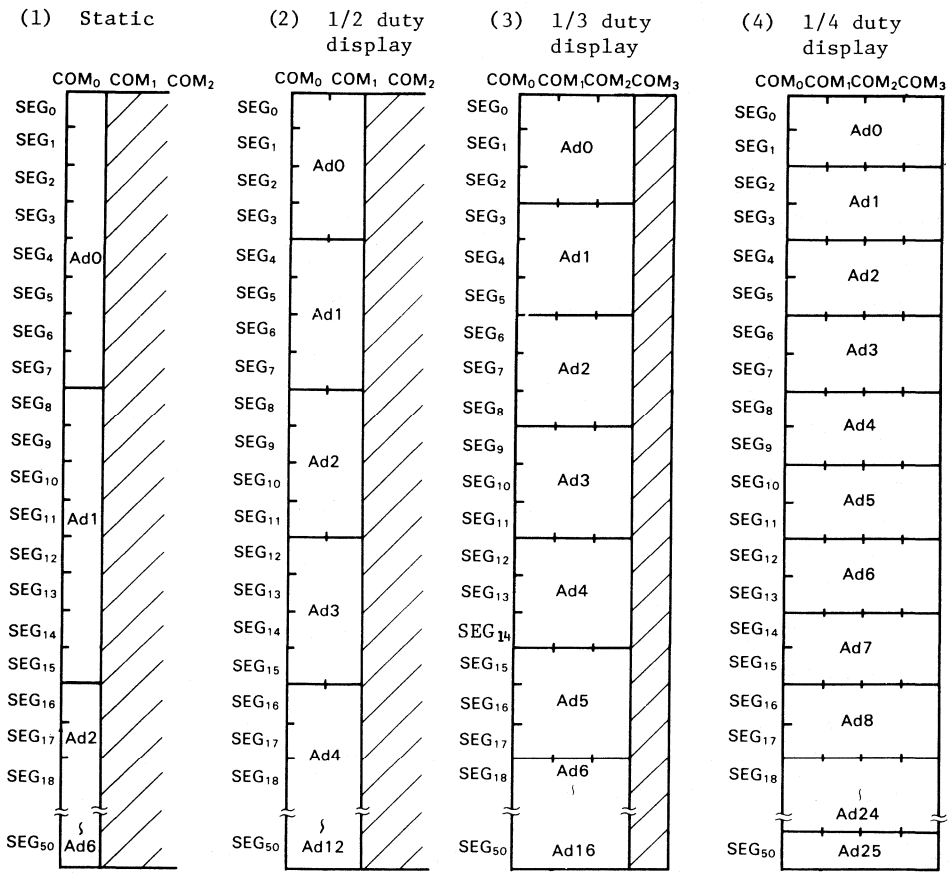


Fig. 8 Allocation of Digit (HD61602)

(1) Static display

	COM_0
SEG_{8n}	Bit 7
SEG_{8n+1}	6
SEG_{8n+2}	5
SEG_{8n+3}	4
SEG_{8n+4}	3
SEG_{8n+5}	2
SEG_{8n+6}	1
SEG_{8n+7}	Bit 0

(2) 1/2 duty display

	COM_0	COM_1
SEG_{4n}	Bit 7	6
SEG_{4n+1}	5	4
SEG_{4n+2}	3	2
SEG_{4n+3}	1	Bit 0

(3) 1/3 duty display

	COM_0	COM_1	COM_2
SEG_{3n}	Bit 7	6	
SEG_{3n+1}	5	4	3
SEG_{3n+2}	2	1	Bit 0

(4) 1/4 duty display

	COM_0	COM_1	COM_2	COM_3
SEG_{2n}	Bit 7	6	5	4
SEG_{2n+1}	3	2	1	Bit 0

Fig. 9 Bit Assignment in an Adn (HD61602)

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

< HD61603 Display RAM >

The HD61603 has an internal display RAM as shown in Fig. 10. Display data is stored in the RAM and output to the segment output terminal.

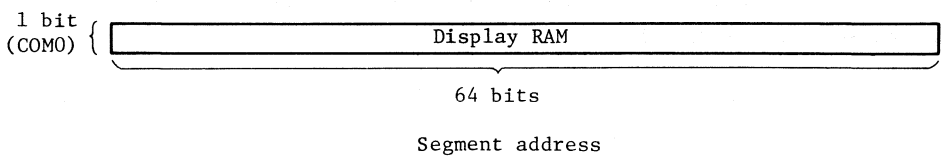


Fig. 10 Display RAM (HD61603)

● Reading Data from Display RAM

Each bit of the display RAM corresponds to each LCD segment. The data at segment address SEGn is output to segment output SEGn terminal. Fig. 11 shows an example of the correspondence between the display RAM bit and the display pattern when a 7-segment type LCD is connected.

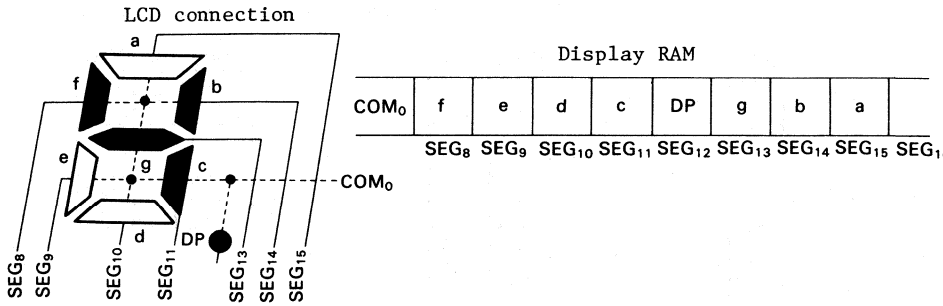


Fig. 11 Example of Correspondence between Display RAM Bit and Display Pattern (HD61603)

● Writing Data into Display RAM

Data is written into the display RAM in the following two methods:

(1) Bit manipulation

Data is written into any bit of RAM on a bit basis.

(2) Static display mode

8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in Fig. 12. When data is transferred from a microcomputer, four 4 bit data are needed to specify the digit address and an 8-bit display data. Fig. 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

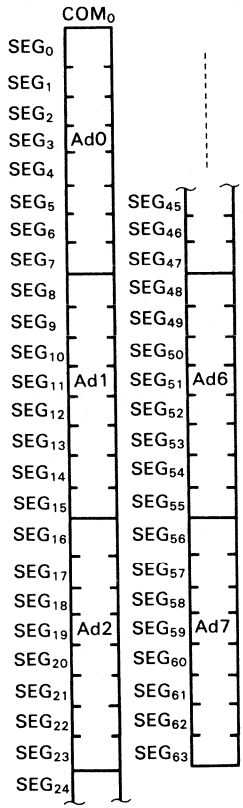


Fig. 12 Allocation of Digit (HD61603)

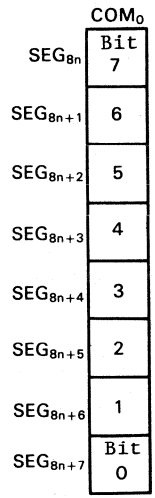


Fig. 13 Bit Assignment in an Adn (HD61603)

In the bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

■ Operating Modes

< HD61602 Operating Modes >

The HD61602 has the following operating modes:

(1) LCD drive mode

Determines the LCD driving method.

(a) Static drive mode

LCD is driven statically.

(b) 1/2 duty drive mode

LCD is driven at 1/2 duty and 1/2 bias.

(c) 1/3 duty drive mode

LCD is driven at 1/3 duty and 1/3 bias.

(d) 1/4 duty drive mode

LCD is driven at 1/4 duty and 1/3 bias.

(2) Data display mode

Determines how to write display data into the data RAM.

(a) Static display mode

8-bit data is written into the display RAM according to the digit in the static drive.

(b) 1/2 duty display mode

8-bit data is written into the display RAM according to the digit in the 1/2 duty drive.

(c) 1/3 duty display mode

8-bit data is written into the display RAM according to the digit in the 1/3 duty drive.

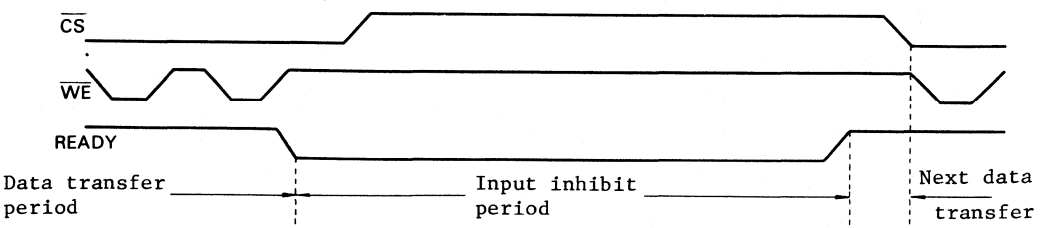
(d) 1/4 duty display mode

8-bit data is written into the display RAM according to the digit in the 1/4 duty display drive.

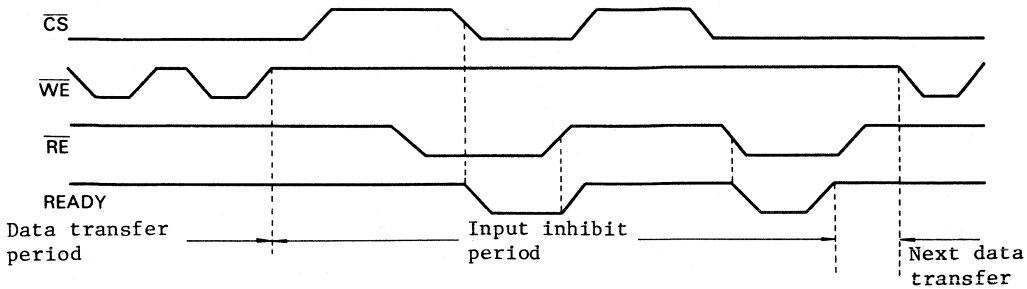
(3) READY output mode

Determines the READY output timing.
After data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when the READY is output can be selected from the following two modes:

(a) READY is always available.



(b) READY is available by $\overline{CS}$ and $\overline{RE}$.



(4) LCD OFF mode

In this mode, the HD61602 stops driving LCD and turns it off.

(5) External driving voltage mode

A mode for using external driving voltage (V1, V2 and V3).

The above 5 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

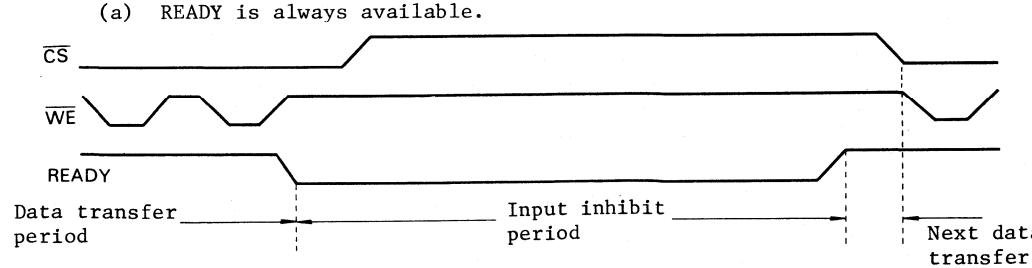
< HD61603 Operating Modes >

The HD61603 has the following modes:

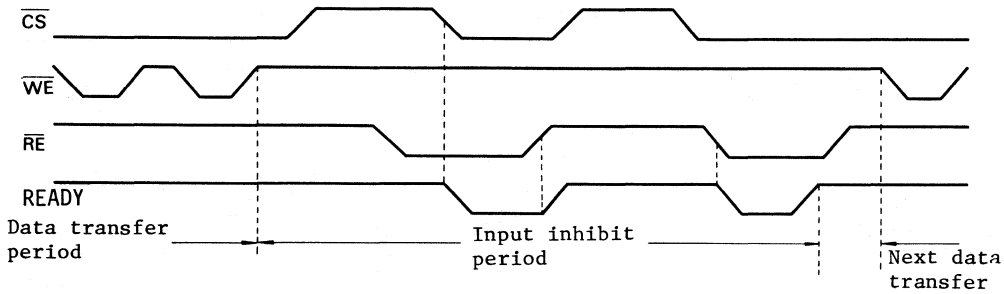
(1) READY output mode

Determines READY output timing.
After data set is transferred, the data is processed internally.
The next data cannot be acknowledged during the processing period.
The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:

(a) READY is always available.



(b) READY is available by $\overline{CS}$ and $\overline{RE}$.



(2) LCD OFF mode

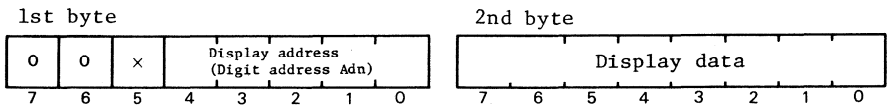
In this mode, the HD61603 stops driving LCD and turns it off.

■ INPUT DATA FORMATS

HD61602 Input Data Formats

Input data is composed of 8 bits × 2. Input them as 2-byte data after READY output is changed from "Low" to "High" or "Low" pulse is entered into $\overline{RE}$ terminal.

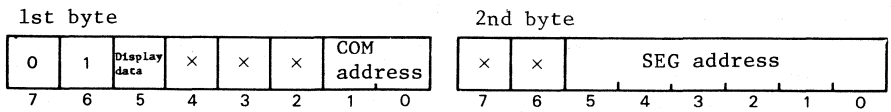
(1) Display data (Updates display on an 8-segment basis.)



(i) Display address: Digit address Adn in accordance with each display mode.

(ii) Display data : Pattern data that is written into the display RAM according to each display mode and the address.

(2) Bit manipulation data (Updates display on a segment basis.)

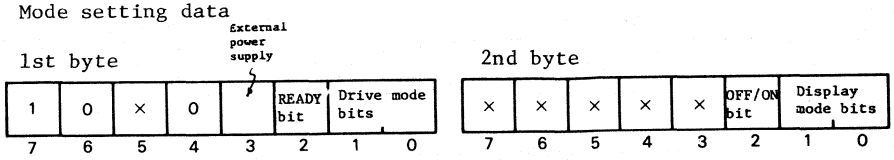


(i) Display data : Data that is written into 1 bit of the specified display RAM.

(ii) COM address : Common address of display RAM.

(iii) SEG address : Segment address of display RAM.

(3) Mode setting data



(i) Display mode bits : 00; Static display mode
01; 1/2 duty display mode
10; 1/3 duty display mode
11; 1/4 duty display mode

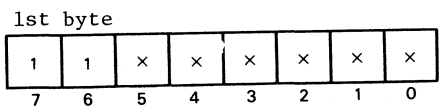
(ii) OFF/ON bit : 1; LCD OFF ("1" is set when SYNC is entered.)
0; LCD ON

(iii) Drive mode bits : 00; Static drive
01; 1/2 duty drive
10; 1/3 duty drive
11; 1/4 duty drive

(iv) READY bit : 0; READY outputs "0" only while $\overline{CS}$ and $\overline{RE}$ is "0". ("0" is reset when SYNC is entered.)
1; READY outputs "0" regardless of $\overline{CS}$ and $\overline{RE}$.

(v) External power supply bit : 0; Driving voltage is generated internally.
1; Driving voltage is supplied from external. ("1" is set when SYNC is entered.)

(4) 1-byte instruction

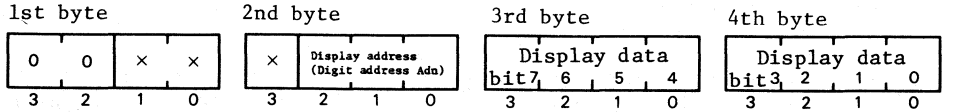


The first data (first byte) is ignored when the bit 6 and bit 7 in the byte are "1".

< HD61603 Input Data Formats >

Input data is composed of 4 bits × 4. Input them as four 4 bit data after READY output is changed from "Low" to "High" or "Low" pulse is entered into $\overline{RE}$ terminal.

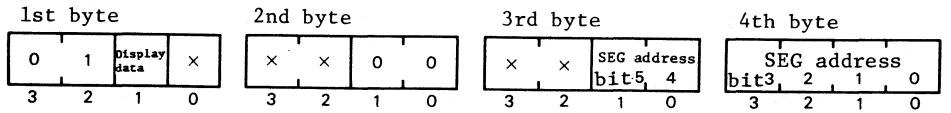
(1) Display data (Updates display on an 8-segment basis.)



(i) Display address: Digit address Adn shown in Fig. 12.

(ii) Display data : Pattern data that is written into the display RAM as shown in Fig. 13.

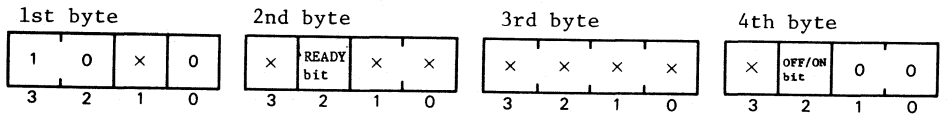
(2) Bit manipulation data (Updates display on a segment basis.)



(i) Display data : Data that is written into the 1 bit of the specified display RAM.

(ii) SEG address : Segment address of display RAM (segment output).

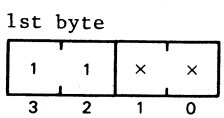
(3) Mode setting data



(i) OFF/ON bit : 1; LCD OFF ("1" is set when SYNC is entered.)
0; LCD ON

(ii) READY bit : 0; READY outputs "0" only while $\overline{CS}$ and $\overline{RE}$ are "0". ("0" is reset when SYNC is entered).
1; READY outputs "0" regardless of CS and RE.

(4) 1-byte instruction



The first data (4 bits) is ignored when the bit 3 and 2 in the data are "1".

■ HOW TO INPUT DATA

< How to Input HD61602 Data >

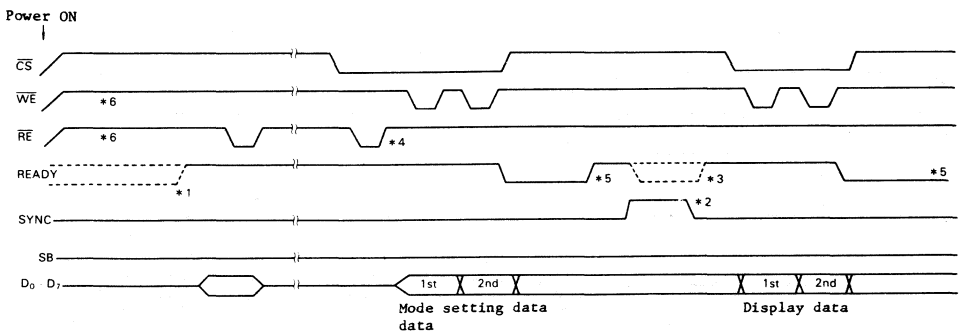
Input data is composed of 8 bits × 2. Take care that the data transfer is not interrupted. Because the first 8-bit data is distinguished from the second one depending on the sequence only.

If data transfer is interrupted or at the power ON the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

(1) Set $\overline{CS}$ and $\overline{RE}$ inputs in "Low" (no display data changes).

(2) Input 2 or more "1-byte instruction data" which bit 7 and 6 are "1" (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D0 to D7) is similar to that of static RAM such as HM6116. An access of the LSI can be made through same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and Fig. 14.



*1: READY output is indefinite during 12 clocks after the oscillation start when power ON (clock: OSC_2 clock).

*2: "High" pulse should be applied to SYNC terminal when using two or more chips synchronously.

*3: In the mode in which READY is always available, READY output is indefinite while "High" is being applied to SYNC.

*4: Reset the byte counter after power ON.

*5: READY output period is within 4.5 clocks in the mode setting operation and bit manipulation or within 11.5 clocks when the display data (8 bits) is updated.

*6: Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.

Fig. 14 Example of Data Transfer Sequence

< How to Input HD61603 Data >

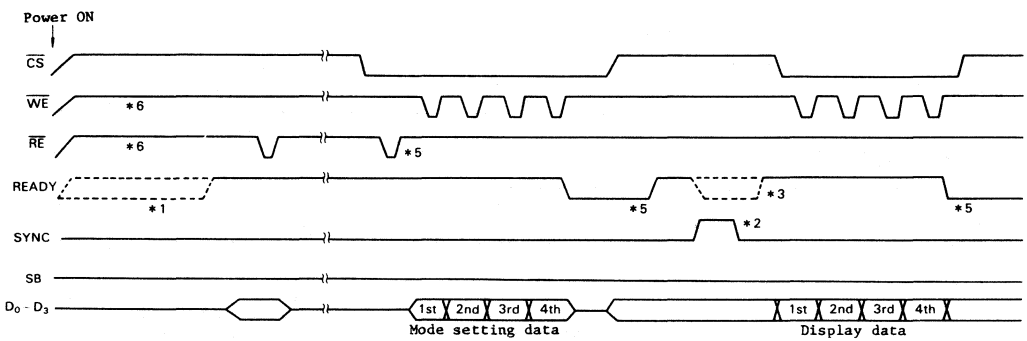
Input data is composed of 4 bits × 4. Take care that data transfer is not interrupted. Because the first 4-bit data to the fourth 4-bit data are distinguished from each other depending on the sequence only.

If data transfer is interrupted or at the Power ON, the following two methods can be used to reset the count of the number of data (count of the first 4 bit data to the fourth 4-bit data):

(1) Set $\overline{CS}$ and $\overline{RE}$ in "Low".

(2) Input 4 or more "1-byte instruction" data (4-bit data) which bit 3 and 2 are "1" (display data may change).

The data input method via data input terminals ($\overline{CS}$, $\overline{WE}$, D0 to D3) is similar to that of static RAM such as HM6116. An access of the LSI can be made through the same bus line as ROM and RAM. When output ports of a microcomputer are used for an access, refer to the timing specifications and Fig. 15.



*1: READY output is indefinite during 12 clocks after the oscillation start when power ON (clock: OSC_2 clock).

*2: "High" pulse should be applied to SYNC terminal when using two or more chips synchronously.

*3: In the mode in which READY is always available, READY output is indefinite while "High" is being applied to SYNC.

*4: Reset the 4-bit data counter after power ON.

*5: READY output period is within 4.5 clocks in the mode setting operation and bit manipulation or within 11.5 clocks when the display data (8 bits) is updated.

*6 Connect a proper pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.

Fig. 15 Example of Data Transfer Sequence

■ STANDBY OPERATION

Standby operation with low power consumption can be activated when terminal SB is used. Normal operation of the LSI is activated terminal SB is "Low" level and the LSI goes into the standby state when terminal SB is "High" level. The standby state of the LSI is as follows:

(a) LCD driver is stopped and no driving voltage is generated (LCD are off).

(b) Display data and operating mode are held.

(c) The operation (in which READY is outputting "Low") during display change is suspended. In this case, READY outputs "High" within 10.5 clocks or 4.5 clocks after release from the standby mode.

(d) Oscillation is stopped.

When this mode is not used, connect terminal SB to V_{SS}.

■ MULTI-CHIP OPERATION

When a LCD is driven with two or more chips, the driving timing of LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is "High", the LCD driver timing circuit is reset. Apply "High" pulse to the SYNC input after the operating mode is set.

A "High" pulse to the SYNC input causes the change of the mode setting data (The OFF/ON bit is set and the READY bit is reset. See (3) mode setting data in "Input Data Formats".). Transfer the mode setting data into the LSI after every SYNC operation.

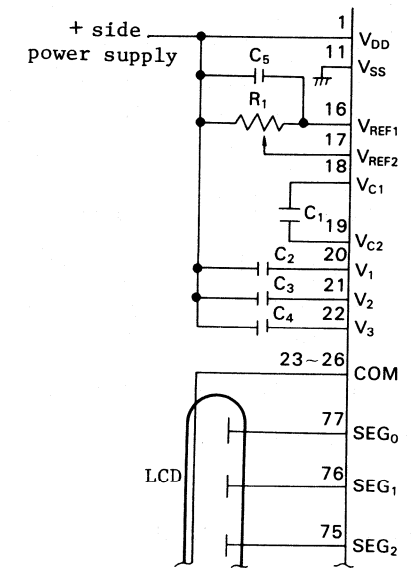
If a Power ON RESET signal is applied to the SYNC terminal, the LCD can be off-state when the Power is turned on.

When SYNC input is not used, connect terminal SYNC to V_{SS}.

■ LIQUID CRYSTAL DISPLAY DRIVING VOLTAGE GENERATION CIRCUIT (HD61602)

● When Internal Driving Voltage is Used

As shown in Fig. 16, attach capacitances C1 to C4 for boosting circuit and a half-fixed resistor R1 for setting LCD driving voltage. Adjust R1 according to the required LCD driving voltage.

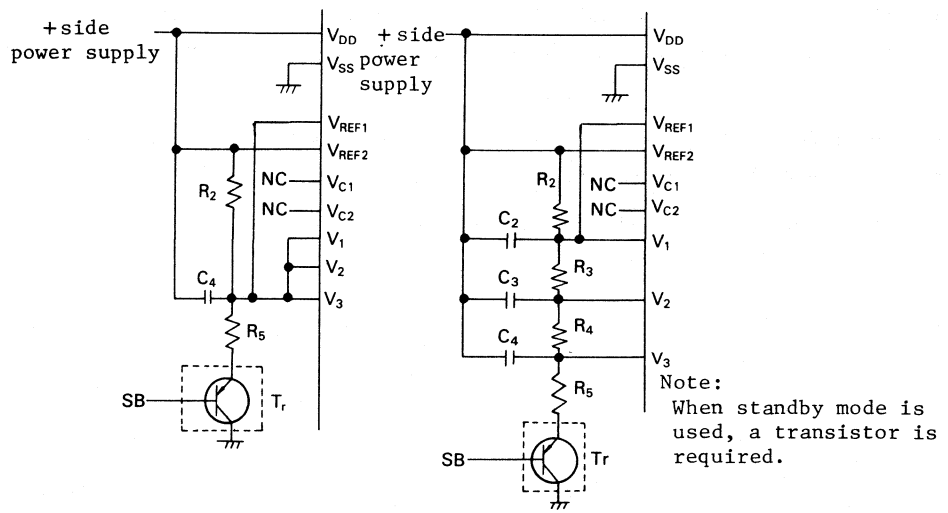


R1 = 1MΩ half-fixed resistor
C1 = 0.3μF C2∿C4 = 0.3μF

Fig. 16 An Example when Internal Driving Voltage is Used

● When External Driving Power Supply is Used

As shown in Fig. 17, the LCD driving voltage is supplied by an external power supply with external resistors and capacitors.



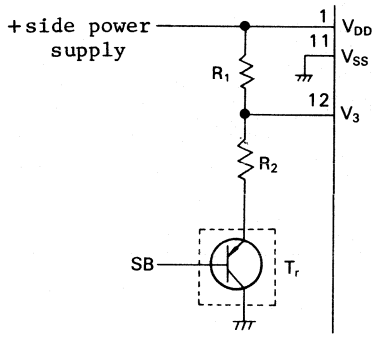
Note:
When standby mode is used, a transistor is required.

(i) Static drive (ii) 1/2, 1/3, 1/4 duty drive

Fig. 17 An Example when External Driving Voltage is Used

■ LIQUID CRYSTAL DISPLAY DRIVING VOLTAGE (HD61603)

As shown in Fig. 18, apply LCD driving voltage from the external power supply.



Note:
When standby mode is used, a transistor is required.

Fig. 18 Example of Driving Voltage Generator

■ OSCILLATION CIRCUIT

●When Internal Oscillator Circuit is Used

When the internal oscillator circuit is used, attach an external resistor R_{OSC} as shown in Fig. 19.

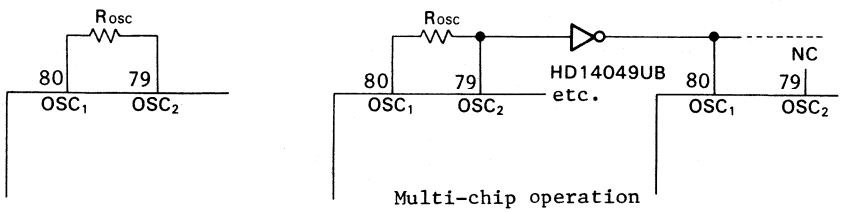


Fig. 19 Example of Oscillator Circuit

●When External Clock is Used

When an external clock of 100kHz with CMOS level is provided, terminal OSC1 can be used for the input terminal. In this case, open terminal OSC2.

APPLICATIONS

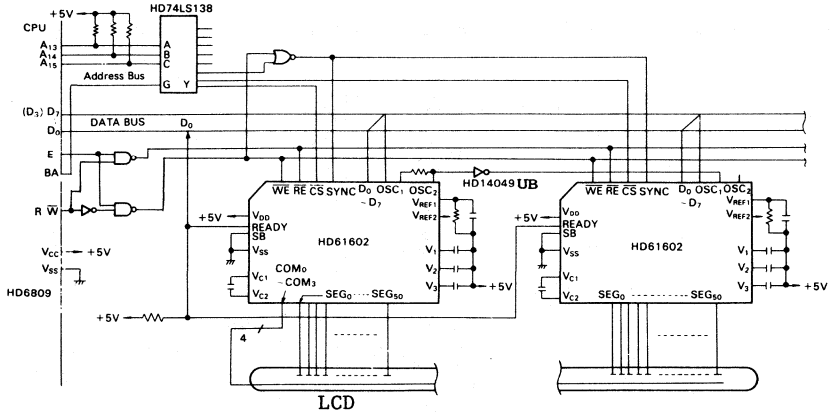


Fig. 20 Example (1)

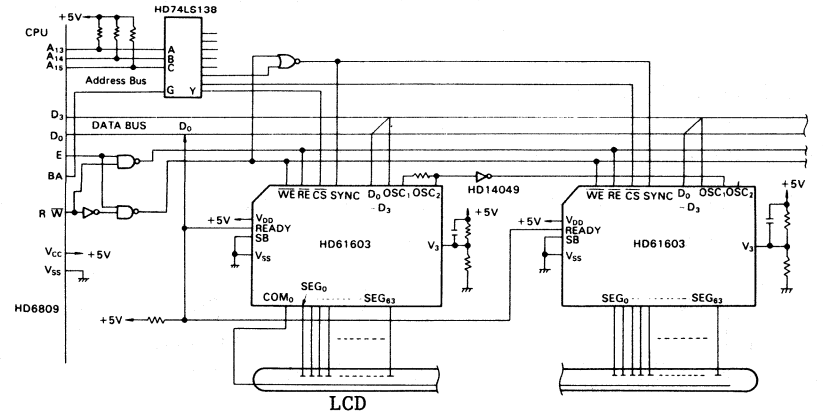


Fig. 21 Example (2)

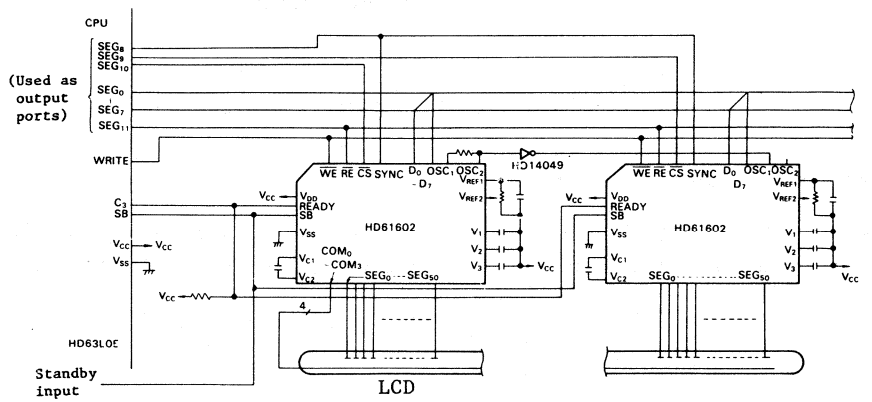


Fig. 22 Example (3)

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